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SOLUTION PROCESSED THIN FILM TRANSISTORS FOR ORGANIC LIGHT EMITTING DIODE BACKPLANE

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Abstract

Solution processed electronics is a low cost device fabrication methodology that has gained research interest over past two decades. The continuous rising of this field is due to the increasing number of discoveries and research work being done alongside in material science domain, providing it new alternatives and techniques to enhance the device performance. The main idea of solution processed electronics is to fabricate a large number of devices that show optimal performance in an inexpensive way, and trying to eliminate certain processes and infrastructures that need a lot of expenditure like high class cleanrooms. A parallel motive to undertake this research is also to develop devices using such materials that can enable us to create a flexible and a transparent device.

These type of devices are the main interest of the research. Focused on understanding and designing new fabrication methodology for Thin Film Transistors (TFT) is the key objective of this research. During the experimentation period of this research project, various materials and device structures were tried and tested to produce an optimized TFT that will be used in the backplane of an OLED and will be used to switch the OLED on and off. Hence the requirements for the output parameters of the TFT were known in the beginning in accordance with the OLED it needs to switch. The transistor parameters like ON current, OFF current, gate leakage, threshold voltage, mobility and ON/OFF ratio were optimized.

The device architecture was also the research focus and two designs were developed, tested and optimized. These different designs were aimed at different type of applications of the OLED, which the TFT will be driving. The first type was the segmented device and the second type was the pixelated device. The basic difference between the two devices is in the size, but in order to fabricate the devices, the process used was a lot different from each other. For the segmented device, conventional thin film deposition techniques were used like spin coating and physical vapor deposition. For the pixelated device in addition to the conventional techniques, some additional processes were also used like photolithography, making it more complex compared to the segmented device.

Acknowledgements

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Finally I would like to thank my parents and my brother for their endless encouragement and love, and for offering me an opportunity to pursue my dreams.

Gupta Mihir

January 2015

"I just try to have fun, it's about having a good time."

— Lemmy Kilmister

Table of Contents

“The first principle is that you must not fool yourself and you are the easiest person to fool.”

— Prof Richard Feynman

List of Figures

List of Tables

Acronyms

AOS	Amorphous Oxide Semiconductors
a-Si:H	Amorphous – Silicon : Hydrogen
OLED	Organic Light Emitting Diode
TFT	Thin Film Transistor
FET	Field Effect Transistor
ZTO	Zinc Tin Oxide
IZTO	Indium Zinc Tin Oxide
ITO	Indium Tin Oxide
UV	Ultra Violet rays
PEDOT:PSS	Poly(3,4-ethylenedioxythiophene) Polystyrene Sulfonate
MBE	Molecular Beam Epitaxy
PLD	Pulsed Laser Deposition
CVD	Chemical Vapour Deposition
PET	Polyethylene terephthalate
PEN	Polyethylene 2,6-naphthalate
JFET	Junction Field Effect Transistor
MESFET	Metal Semiconductor Field Effect Transistor
SiO_2	Silicon Dioxide
E_i	Intrinsic Fermi Level
E_f	Fermi Level
CBM	Conduction Band Minimum
VBM	Valance Band Maximum
TCO	Transparent Conductive Oxide
PVP	Poly(4-vinylphenol)
PMMA	Poly(methyl methacrylate)
PMF	poly(melamine-co-formaldehyde)
PGMEA	Propylene Glycol Methyl Ether Acetate

Dissertation Outline

The object of this dissertation is to investigate two different Thin Film Transistor designs on transparent substrate, develop low cost fabrication process and optimize them to meet the specifications as to drive and switch OLEDs.

The thesis is divided into 6 chapters. **Chapter 1** is the introductory chapter giving a brief account of the background, current work and the experiments done in this thesis. It also includes the theoretical and practical understanding width wise in the fields associated with Thin Film Transistors and materials. **Chapter 2** deals with the literature survey, and includes all the work being done in the past till today in the field of TFT and conductive oxides. **Chapter 3** explains the theory behind the working and the operation of field effect devices like MOSFET and TFT, and explains the analysis of I-V characteristics. The **chapter 4** includes the work done in this thesis and the experimental part for both the TFT designs. Thereafter the **chapter 5** is the most important chapter and explains the result and the analysis portion of the experiments done. Finally **chapter 6** concludes the results and gives a short account of the possibilities of the future work that can be carried out.

Chapter 1: Introduction

Solution based and printed electronics is a unique branch in Nanoelectronics that complements the conventional Silicon based technology, facilitating low cost solutions to electronic devices and circuits on transparent and/or flexible substrates. This field is continuously revolutionizing and improvising to provide everyday need based 'smart' solutions that are being seen everywhere. Ranging from highly complicated medical sensors and devices to ubiquitous entertainment gadgets and displays, printed and solution based electronics has a large application area. Displays that can be folded like paper, medicines injected in the body through painless patches, solar cells, various kinds of sensors to detect gases, food spoilage, leakage etc. are some of the most popular applications of printed electronics.

All these application can be successfully implemented if the industry can profitably mass produce backplane driver and switching circuits to make these sensors and displays work effectively. These backplane circuits must have the same physical characteristics as that of the device so as to facilitate best usage and compatibility. For example, backplane driver circuit for a skin compatible flexible gadget must also be flexible and transparent for successful integration with the device. Hence here we have the main challenge to overcome these barriers.

The backplane is made up of Thin Film Transistors (TFTs) that switches and drives the device. These TFTs can be manufactured by various methods and various materials can be used depending upon the physical and electrical characteristics of the device it will drive and switch. Most popular methods include solution based processing, inkjet printing and screen printing.

For applications like displays and OLEDS, we need transparent TFT panel as driver circuitry. Transparent conductive oxides have received much attention in the recent years for their suitable properties to be used for displays and flexible electronics. Transparent conductors like Indium Tin Oxide (ITO) has been commercially in use for quite some time now [1]. A lot of research is being done on Zinc Oxide and Indium Tin Oxide. These materials can be used for large area electronics and have huge potential also because they are cheap. An effort is also being made to reduce

the cost of the processing as well. Hence the processes like screen printing and inkjet printing that can reduce the cost by elimination the need of photolithography and expensive cleanrooms.

1.1 Microelectronics and Macroelectronics

Microelectronics as the word suggests includes the study of devices and circuits in micron range or below. It is mainly developed using Silicon as semiconductor and its focus is on developing cheap, high efficiency and high yield devices that can be used for applications like computing, communication devices, memory storage etc. Hence more and more stress is laid on making the device work faster at low operating voltage and at cheaper price. The state-of-the are devices in this domain have gate length of 14 nm, and they are currently in high volume manufacturing by Intel [2].

Macroelectronics on the other hand although lays stress on the performance and yield too, but the real focus for it is to make devices as cheap as possible, for applications that do not need high sophisticated circuitry. These applications include display technology, use and throw electronics including detectors/sensors, biomedical devices that are required to be discarded after single use and similar devices. It is proposed that the fabrication of such devices can further be made cheaper if they will not involve conventional Silicon manufacturing techniques like lithography, reactive ion etching, high temperature annealing etc. Eliminating these processes will eliminate the need for a high class cleanroom and the expenditure associated with it. Hence it is important to make these devices very cheap so they can fall under affordable limit, with a trade-off with the performance, technology and efficiency.

Another advantage macroelectronics seeks as compared to microelectronics is its ability that it can fabricate transparent devices and also flexible ones, which is not possible to achieve with conventional Silicon technology. Hence these are the possible areas that are needed to be explored in macroelectronics.

1.2 Current State with Solution Based Electronics

Solution based electronics unlike conventional Silicon based electronics makes use of bottoms up approach to fabricate devices. Conventional Silicon fabrication

methodology makes use of top-bottom approach in which the Silicon substrate is used as a base, and lithography and etching is performed to get the desired structure. The Silicon substrate is first coated with a photoresist by spin coating. Then the top part of the wafer which is coated with photoresist is covered with a mask and exposed to Ultraviolet light (UV) of specific wavelength to modify the exposed portion of the mask. Subsequently the wafer is then selectively etched or dipped in a developer solution to remove the unwanted portion of the masked wafer in order to obtain a pattern. This pattern is then used as a mask in itself for further processing. This is a generalized process for Photolithography to obtain a pattern and involves a lot of steps depending on the pattern and the material used. On the contrary, then we talk about printed electronics, we need just on single step and that would be direct printing of the pattern on the substrate. If it is screen printing, then the substrate is places below a mesh (that hold a pattern), and the ink or the paste is patterned on the substrate directly via the small holes in the mesh. If it is ink jet printing, then the substrate is kept on the ink jet printer's paten and a jet nozzle continuously drops ink to create the desired pattern. This pattern can then be forwarded for subsequent annealing and processing. Hence the overall process is simpler when compared with conventional fabrication and processing.

As we can see that solution based electronics is a much faster way to make electronics circuits and one can directly make patterns without the need to involve multiple steps. This is of a great advantage when we are concerned with macro electronics as opposed to microelectronics. For macroelectronics, the main issue is cost-effectiveness whereas for microelectronics although cost is an issue but the industry is also much concerned about the performance and the yield of the process. Hence even if there is degradation in performance as compared to conventional devices, they can still be used for the display, driver circuit and similar applications, but the important criterion is that they must be manufactured cheap.

Although there are some compromises that are needed to be considered when using solution based electronics. The main issues are with the device performance and device construction and substrate preparation (surface adhesiveness). The device performance including parameters like mobility, On-Off ratio and Threshold Voltage are not up to the mark as achieved with conventional technology. The main reason

for this is suspected to be the non-uniformity in the solution deposition while printing, the issues associated with the surface adhesiveness, residual solution and gas trapping while annealing. These variables influence the performance of the devices varying their parameters with each batch. For the device construction issue, the minimum feature size is a constraint. The line width obtained by photolithography is substantially less than obtained with printing. This limits the application areas for the device and hence increasing the cost of production.

1.3 Solution process based materials

As mentioned earlier there has been substantial amount of research going on for materials that are compatible with solution processing. Semiconductor inks like Zinc Oxide (ZO), Indium Zinc Tin Oxide (IZTO) etc. have been researched extensively and good reports have been published on improved transistor parameters like mobility and On-Off ratio. Printing is not only done for the semiconductor but also for conductors and for making electrical components. Carbon is very well known to be screen printed and used both as electrode as well as a resistor [3]. Other materials like metal nanoparticles (Au, Ag, and Cu) can be inkjet printed to form conductive paths. Hence in this way we can make use of these materials to form a transistor that is totally based on solution based processing. Moreover, a good amount of research is also going to make transparent circuits. Materials like IZTO and ZO are known to be transparent semiconductors which are a very good choice for such circuits. For electrodes and conductive paths there have been reports on using materials like PEDOT:PSS and ITO by inkjet printing [4]. Another alternative is nanoparticles that offer better conductive paths and can be inkjet printed.

The above mentioned semiconductor inks are mostly inorganic materials. There also have been a great deal of research on organic semiconductors, but due to their instability in air and relatively poor mobility, they suffer a lag compared to inorganic semiconductors.

1.4 Inorganic and Organic Materials

As of today we can already see devices made of organic materials like cell phone displays and television displays. They are made of Organic Light Emitting Diodes (OLEDs) which are available as a commercialised device. Hence a lot of research

has already been conducted on organic materials and they have been understood well as compared to inorganic materials. Despite some disadvantages like low mobility, organic materials are easy to print and the annealing temperature needed is low, which reduces the cost of production. When comparing inorganic materials with organic, one can see that inorganic oxides have higher mobility and are stable in air, which is a big advantage. Also not much research has been done on inorganic oxide materials to be used as conductors or semiconductors. Hence there is a wide scope of possibilities in case of inorganic oxides.

Usually we find that the inorganic oxides are n-type semiconductors like Zinc Oxide (ZO), Zinc Tin Oxide (ZTO), Indium Zinc Oxide (IZO) etc. where as in case of organic materials, they usually are p-type semiconductors due to strong trapping of electrons but not holes [5].

1.5 Solution Processed Transparent Conductive Oxides

The solution processing of conductive oxides can be done in the following three ways:

- Nanoparticles
- Nanowires
- Solution deposited thin film

1.5.1 Nanoparticles

This methodology involves suspension of nanoparticles in a solution and then either spin coating the solution or using inkjet printer to make the pattern. Since the surface area to volume ratio of the nanoparticles is more than that of bulk material, we need lower temperature to anneal the thin film. This is a big advantage since low temperature processing reduces the cost of production and also enables processing on substrates that are flexible and transparent like PET and PEN. On heating the deposited pattern, the nanoparticles fuse together to form a crystalline layer.

1.5.2 Nanowires

The process involved in solution processing of the nanowires is somewhat similar to those involving nanoparticles. Though the case with nanowires should theoretically give better performance as they have better transport characteristics, but due to less

control on the packing density of the wires, the practical result do not match the theoretical speculations.

1.5.3 Solution Deposited Thin Film

This process involves formation of the conductive oxide not externally but directly on the substrate. This is much different from nanoparticle and nanowire deposition in the way that nanoparticles and wire are already processed before their deposition, but in this case the reaction takes place on the substrate directly. This process has its own pros and cons. A good thing about this process is that the quality and uniformity obtained is much higher than nanoparticles or wires. Although as for the reaction to take place, most of the reactions for the formation of conductive oxides need high temperatures (300 - 600 °C), hence making the process unfavourable for flexible substrate that have low melting point, and also increasing the cost of production. This process can be carried out in the following major forms:

1. Spin coating [6]
2. Dip Coating [7]
3. Sol Gel [8]
4. Spray Pyrolysis [9]

The experiments I performed for my thesis work were done using spin coating to fabricate Thin Film Transistors (TFTs) and Zinc Tin Oxide (ZTO) as transparent conductive oxide for semiconductor thin film.

1.6 Carrier Transport in Amorphous Metal Oxides

Amorphous Semiconductors have low mobility when compared with polycrystalline materials. But amorphous materials still have some characteristics that makes them still a viable candidate for certain types of transistors, where mobility is not a concern. These properties include uniformity of device characteristics and low temperature processing [10] [11]. These properties make them useful for our purpose which is for OLED backplane, flexible electronics and also use-and-throw electronic sensors.

Like all the solids, band structures are a good source of information for understanding the electronic properties of metal oxides. But due to complex

interaction of the metal orbitals with Oxygen orbitals, the electronic structure of the metal oxides gets complicated. Also there increases a difference in the conduction properties of electrons and holes for these materials. The band gap in case of Silicon if the energy difference between the σ* - σ levels. These are special hybrid orbitals in conduction band minima and valance band maxima corresponding the anti-bonding and bonding states in case of Silicon [11, 12]. Due to this the electronic structure of the metal oxides is different from that of a covalent banded semiconductor. In case of the common conductive metal oxides the conduction band and the valance bands are formed by the ns orbital of the metal and the 2p orbital of the oxygen [13]. Due to this the conduction band minima thus formed is highly spread while the valance band maxima is localized. This further leads to the difference in the electron and the hole effective masses, making electrons lighter therefore associated higher mobility for n-type devices. It is one of the main reasons why there are more n-type devices as compared to p-type devices.

The low mobility in amorphous semiconductors can be explained when we study the charge carrier mechanism in the material which is done by "Hoping" mechanism that occurs between localized tail-states, which is different from band conduction [14]. The stated low mobility is linked with the intrinsic feature of the chemical bonds. The carrier transport part in semiconductors that feature covalent bonds like a-Si:H use the sp3 orbitals, which are highly directional. Hence if there is any alteration in the bond angle of these sp3 bonds, this changes the electronic states, which leads to high-density deep tail-states.

Although, there are some amorphous semiconductors that have better performance and higher mobility, like Amorphous Oxide Semiconductors (AOS) that have post-transition metal cations attached to Oxygen molecules forming an M-O-M bond structure. The bottom of the conduction band of the AOS with cation electronic configuration $(n\text{-}l)d^{10}\ ns^{0}$ (with $n \geq 4$) is mainly composed of spatially spread metal ns orbital, and because of the uniform spread of the metal ns orbitals, it allows direct overlap among neighbouring orbitals. This property is very useful as the overlapping is not affected by the amorphous nature of the oxide, and the direct overlapping of the metal orbital is large compared to the 2p overlapping of the Oxygen orbitals (Figure 2)[11].

Therefore, in amorphous oxides (without metal cations), the overlapping occurs only between the directional sp3 orbitals, where as in AOS with metal cations, the amorphous nature does not affect the overlapping as the overlapping is between isotropic metal orbitals, hence in this case we obtain higher mobility.

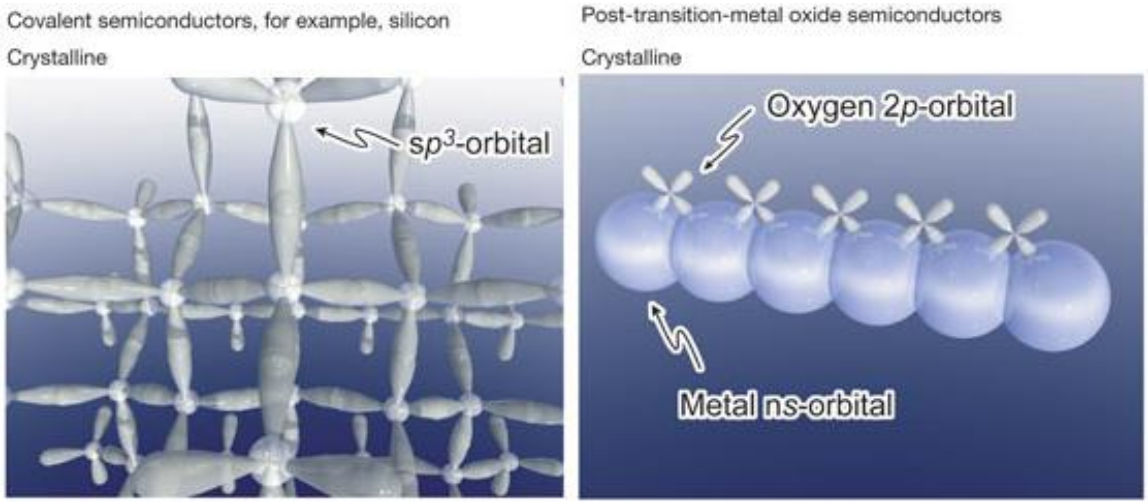


Figure 1: In case of crystalline semiconductors, the overlapping (if covalent) takes place among highly directional sp3 orbitals, and (if with metal ion) takes place between metal ns orbitals which are isotropic. From the figure we can see that the oxygen 2p overlapping is negligible [11]

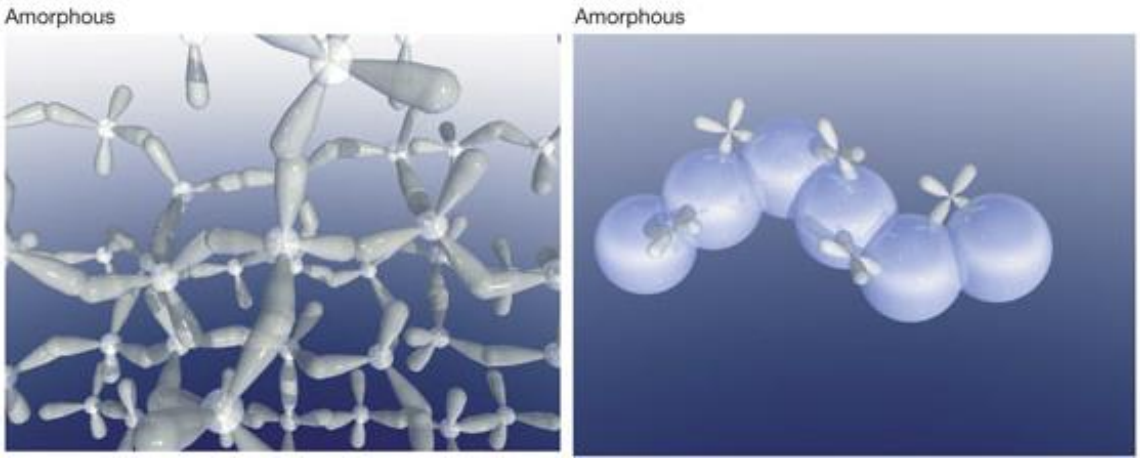


Figure 2: In case of amorphous semiconductors, when overlapping occurs between highly directional sp3 orbitals, there is a huge randomness in overlapping and hence the carrier transportation is inefficient; while in case of amorphous oxide semiconductors with metal cations, the randomness does not affect this overlapping of ns metal orbitals because of their isotropic nature [11]

As discussed earlier, that metal oxides have a complicated electronic structure which makes them semiconductor in nature, but their conductivity is comparatively less mainly because of the wide band gap for the materials, due to which there are

negligible thermal excitations, hence low intrinsic carrier density. So in order to increase the conductivity, other methodologies are adopted like growing n-type materials in oxygen rich environment. This will increase their conductivity making them more metallic in nature. This finding is based on the experiments that found that electrical conductivity of such materials is associated with non-stoichiometry of the metal-oxide system [15]. Therefore Oxygen vacancies are a good source for increasing the conductivities in n-type materials. Similarly for p-type materials, the conductivity is associated with metal interstitials. Although this picture is actually more complex, and the debate is still going on the actual reasons.

Therefore using this special property of AOS with metal cations, the thesis aims to optimize thin film transistor parameters and develop two major types of TFTs for driving and switching OLEDs:

1. Segmented Device: Single large size TFT to drive an $55mm^2$ OLED
2. Pixelated Device: Single micron sized TFT to drive a pixel sized OLED.

The fabrication methodology for both the devices will be different and also the materials used, as the output parameters are different for both the devices. The optimization of the parameters includes ON-OFF Ratio, Sub-Threshold Swing, ON current, OFF Current, Gate Leakage and Mobility. The thesis is aimed to optimize these parameters and finally come up with an optimized process technology for a TFT that can drive and switch respective OLEDs and are compatible with industrial manufacturing standards.

Chapter 2: Literature Survey

The patent for the first Field Effect Transistor was filed in 1926 and then in 1934 by Julius Edgar Lilienfeld and by Oskar Heil respectively [16, 17]. The first reports were actually concept patents demonstrating the novel idea of regulating the current flowing in a material using the effect of transverse electrical field. One of the first patented devices was a metal-semiconductor field-effect transistor MESFET, followed by the metal-insulator-semiconductor field-effect transistor MISFET.

The first practical demonstration of the field effect theory based device and the transistor effect was shown by Shockley and his team at Bell Labs in 1947, after the 20 year old patent by Lilienfeld eventually expired. The first practical semiconductor devices making use of this principle was JFET, and MOSFET, which is the bases of the semiconductor revolution was invented later in 1960 by Dawon Kahng and Martin Atalla.

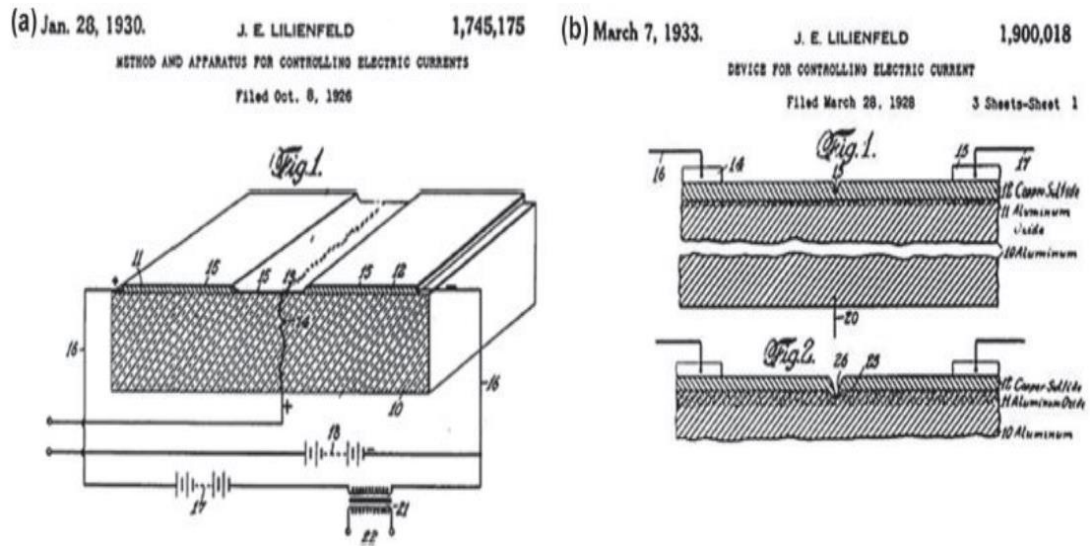


Figure 3: Patent structures by Lilienfeld- MESFET (left) and MISFET (right)

The first working Thin Film Transistor was made by Paul K. Weimer at the RCA Laboratories in 1962. His findings were published in the paper, "The TFT — A New Thin-Film Transistor" in 1962 at the Proceedings of the IEEE, which attracted the attention of the scientists worldwide[18]. Weimer's demonstration was based on an insulated gate structure for a field effect transistor by printing layers of each component: CdS:CdSe (Cadmium Selenide) ink was used to print semiconductor;

Silicate cements was used as dielectric and Hg:In paste was used as conducting electrodes for source and drain.

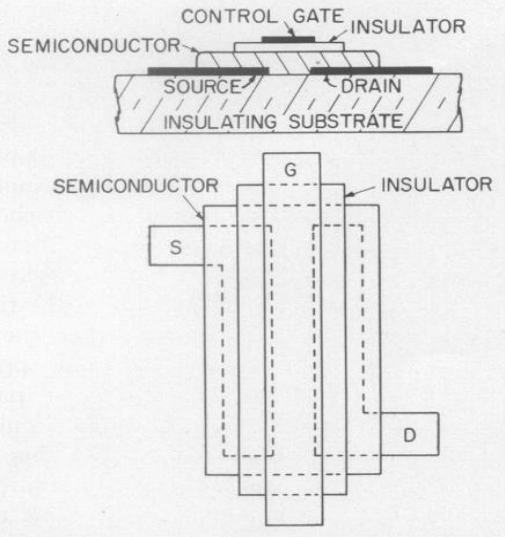


Figure 4: Cross section and also the plan view of an evaporated thin film transistor [18, 19]

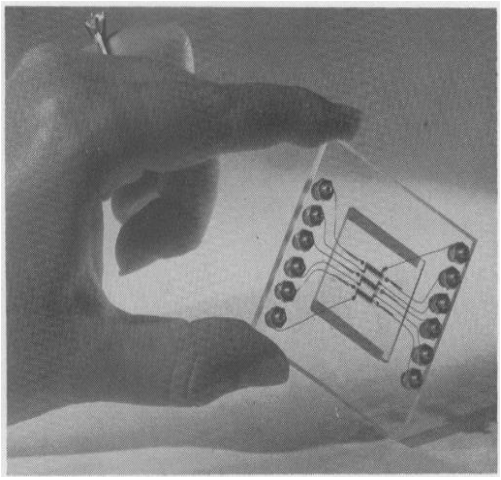


Figure 5: 1 inch square glass slide (attached on a lucite slab)with 3 TFT's fabricated on it [18, 19]

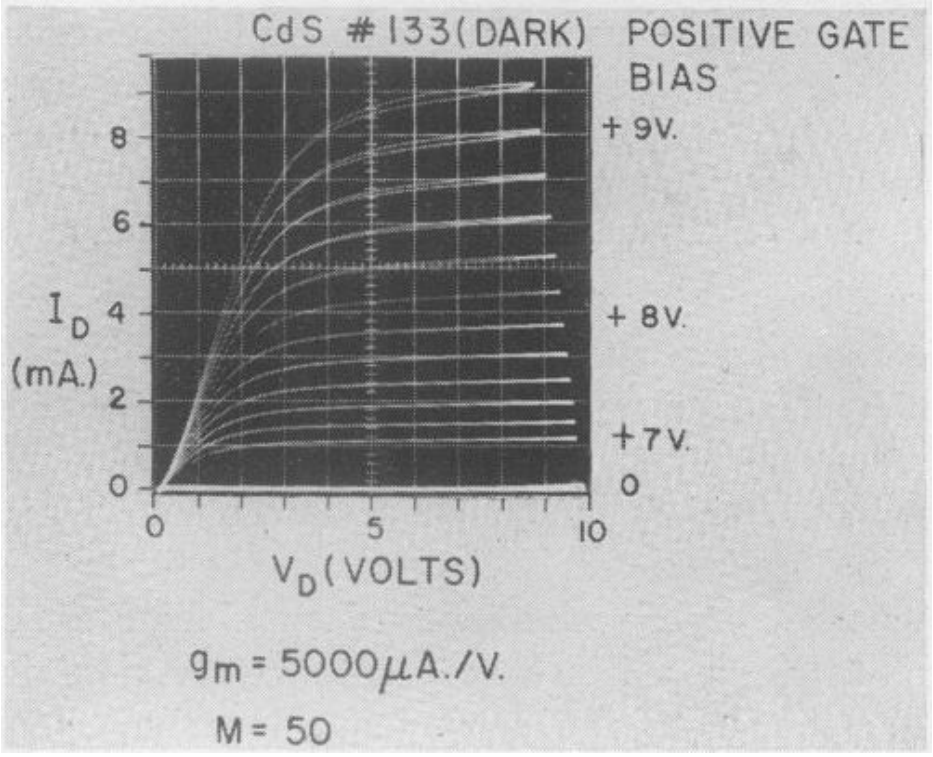


Figure 6: Characteristic curves for an experimental Cadmium Sulfide TFT designed for operation in the "enrichment" mode (Enhancement Mode) [18, 19]

The usage of oxide semiconductors for channel layers in TFTs existed earlier but the performance was not up to the mark. And it was only after 2003 that new and better device performances were reported [20, 21]. These devices with better electrical

characteristics were using ZnO as the semiconductor material for the TFTs and were made by Hoffman et al, Carcia et al. and Masuda et al [22-25]. Hoffman's TFTs were made using Transparent Conducting Oxide (TCO) for the electrodes hence fully optical (as ZnO is also transparent) with optical transmission of 75%, ON/off ratio of 10^7 and average mobility of 2.5 cm^2V^{-1} s^{-1}. Carcia reported TFT fabrication at room temperature by using RF magnetron sputtering giving ON/OFF current ratio of 10^6 and mobility of 2 cm^2V^{-1} s^{-1}. The interesting part is that both the experiments conducted by Hoffman and Carcia gave similar results with mobility better than TFT made using a-Si:H (amorphous Silicon) as semiconductor and more than organic TFTs as well. Results obtained by Masuda were a bit different with average mobility less than 1, ON/OFF ratio of 10^5 and optical transparency of 80%. However, in all the three devices the processing temperature required to anneal the semiconductor was as high as 723 - 873 K in order to get a good performance out of the device. After the demonstration of these results a lot of groups around the world started working on conductive oxides.

Thin Film transistor made using all-polymer technology with insulated gate structure using ink-jet printing was demonstrated for the first time by Sihvonen et al in 2000, inspired by Weimer's TFT [26]. Although the results of the printed TFT were not great, the work is considered as a big leap in printed electronics.

Initially ZnO was used extensively for the TFT fabrication as is it inexpensive and abundant. However, it was suggested that the use of complex materials like GIZO ($InGaO_3(ZnO)_5$) may give better results. The experiment for such device was successfully demonstrated by Nomura et al in 2003 with high mobility of 80 cm^2V^{-1} s^{-1} and ON/OFF ratio of 10^6 [21]. The drawback of this device was that the annealing temperature required to obtain a single crystalline semiconductor layer epitaxially grown on an yttria-stabilized zirconia substrate for GIZO was 1673 K. Thereafter, Nomura et al also made use of flexible substrate to fabricate TFT upon it. This was done by depositing amorphous GIZO as semiconductor by Pulsed laser deposition (PLD) method. This device showed 9 cm^2V^{-1} s^{-1} mobility and ON/OFF ratio of 10^3 mainly because of amorphous nature of the semiconductor leading to non-uniform structure [11]. It was a big step in achieving better mobility when fabrication is done at room temperature; hence since then a lot of studies have been done. Using

precursor solution for making semiconductor films by spin coating was also done by Ohva et al. but the processing temperature was much high of about 1173 K, and obtaining a mobility of 0.2 cm^2V^{-1} s^{-1} and ON/OFF ratio of 10^7 [27]. More studies helped reducing the processing temperature and the deposition method was also changed. In 2011, Making use of the spray pyrolysis technique a mobility of 85 cm^2V^{-1} s^{-1} was achieved with process temperature of 673 K by using Zinc and Lithium acetates for making the precursor solution (Li doped ZnO). This work was done by Adamapoulos et al. and they made us of the bottom gate configuration along with high-k dielectric (ZrO_2) [28]. Adding Tin and Indium to dope ZnO was also used to improve the mobility and reduce the temperature. So IZO and ZTO were used in 2007 to obtain a mobility of 16 cm^2V^{-1} s^{-1} with SiO_2 as dielectric and bottom gate configuration by Chang et al [29-31]. Lower temperature trials were done using GIZO as semiconductor by Yang et al. and Nayak et al. with mobilities of about 8 cm^2V^{-1} s^{-1} and processing temperature of about 473 – 723 K [32-35]. These experiments made use of the hydrothermal and sol get methods to deposit think films of semiconductor materials.

The temperature is a problem because the applications of the TFTs have a huge range and a lot of applications need flexible transparent substrate, all of which have low melting point. Therefore if the processing temperature in high, then it is not possible to print or deposit films on those substrates. To solve this problem, a new approach was tested by Banger et al which involved the use of organic – inorganic metal alkoxide precursor solution to get a layer of amorphous ternary and quaternary oxide semiconductor. This solution processed device gave performance equivalent to device made by sputtering the films, in terms of mobility (10 cm^2V^{-1} s^{-1}) and threshold voltage stability, while keeping the temperature at about 503 K. This process is called sol-gel process and makes use of metal alkoxide precursor solution, with processing capability at lower temperatures [36].

In 2011, a new recipe methodology was used that involved self-energy generation combustion chemistry, which generated localized heat as the chemical reaction being exothermic. This helped to reduce the external requirement for heat to process the fabrication process. M G Kim et al used IO, ZTO and IZO to fabricate TFT with a processing temperature of 473 K [14]. Acetyl acetone or urea was used as fuels and

nitrates as oxidizers to deposit IO by self-combustion method. The TFT obtained in this process had a mobility of 6 $cm^2V^{-1}s^{-1}$. The bottleneck today still remains the processing temperature for the TFT devices. For the dielectric part, it determines the electric field present in the channel and the accumulation of the charges there. The leakage is also determined by the dielectric and cross linking in the dielectric is important to reduce the leakage. Popular dielectrics include Alumina and PVP-PMMA with added cross linking agents.

The surface of the substrate is important as well for the performance of the TFT device. Higher crystalline and smooth surface will scatter less electrons and hence will give better output results.

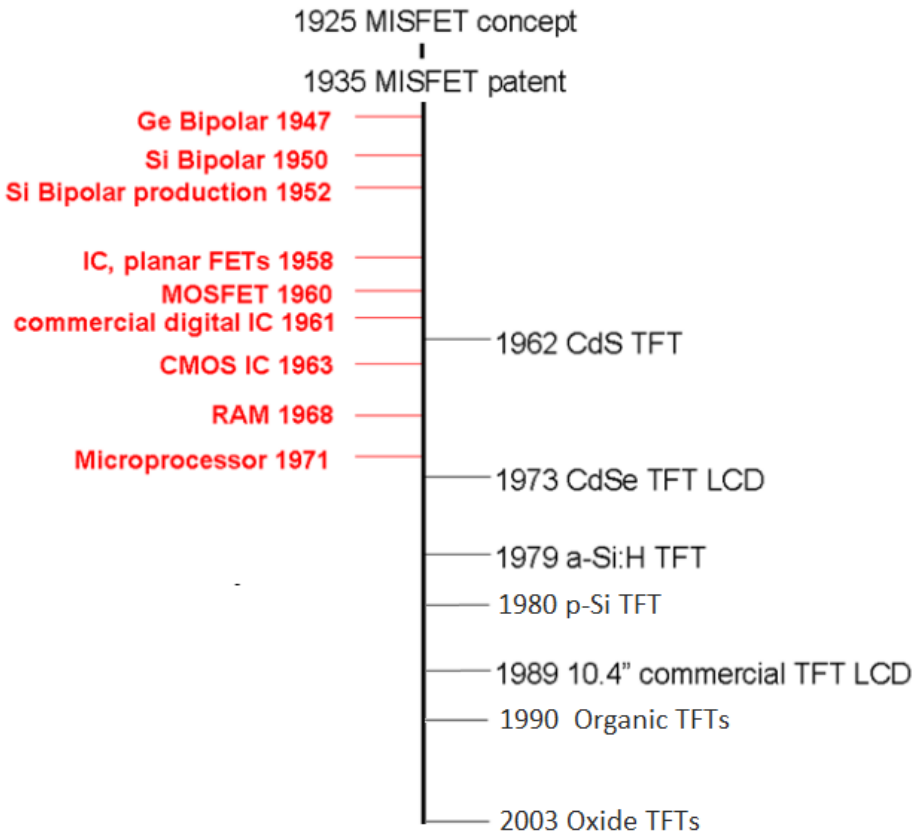


Figure 7: Timeline for Thin Film Transistors along with landmarks in IC development [37]

Table 1: Applications of TFTs [37]

TFT Area	Function	Principles of Operation
Gate Dielectric	pH Sensing	H^+ adsorption in suspended gate dielectric structure
	Memory	PZT gate dielectric
Semiconductor	Gas Sensing	H_2O_2 alcohols, N_2O adsorption on semiconductor layer
	IR Detection	I_d = f(temperature)
Gate Electrode	Gas Sensing	H_2 decomposition on Pd gate electrode
	Bio Sensing	Biomolecule reaction with agents on gate electrode
S/D Electrodes	Protein/DNA Analysis	Contact resistance change due to biomolecule adsorption
	Artificial Retina	Photoconductivity change on attached a-Si:H layer
	X-ray imaging	Scintillator light emission on attached diode
	LEDs	Quantum dot light emission
Structures	Photo sensing	I_{light}/I_{dark} ratio enhanced by split or offset gate
	Memory	Floating-gate dielectric
	Magnetic	Hall effects due to additional electrodes

In this project the TFT fabrication is done in two stages, first one involves TFT fabrication for driving and switching fabricated segmented display and the second involves TFT fabrication for pixelated display. The parameters for the TFT were specified by the industrial collaborators at the beginning of the project and the aim of the project was to fabricate a TFT device to meet those parameters specified by the industry. To reach the desired parameters, various combinations and trials for each later of the TFT were done. Experiments were performed to improvise the substrate, semiconductor, dielectric, source-drain and gate electrodes. Since the final device was to be fabricated on a transparent substrate, Quartz was used for the purpose. The

semiconductor used was Zinc Tin Oxide (ZTO) and experiments were carried out with the Zinc: Tin ratio, recipe methodology and the molarity of the solution. The dielectric used was Poly(4-vinylphenol-co-methyl methacrylate) i.e. PVP-co-PMMA and experiments were carried out with various recipes and additives in PVP-co-PMMA to make it a better dielectric and reduce the leakage. Finally experiments were performed with the source, drain and gate electrodes, to get a smooth surface and to achieve a good ohmic contact with the semiconductor.

Chapter 3: Field Effect Transistor Theory

A Thin Film Transistor works on the principle of field effect theory. It is structured in layers or films of different materials, each of which exhibit their individual properties to combine and work as a transistor. The working principle of a TFT is similar to that of a MOSFET. Lilienfeld mentioned in his first patent about a metal semiconductor field-effect transistor (MESFET). The insulated gate FET (TFT) came later when proposed by Weimer in 1961. The layers in this device were formed through thermal evaporation using shadow mask technique to pattern each layer. For the semiconductor layer cadmium sulphide was used. A TFT is an Insulated-Gate FET with the same basic working principle of a MOSFET but with some structural differences [18].

A MOSFET is a four terminal device: The Silicon substrate body (B), the Source (S), the Drain (D) and the Gate (G). The contact source and drain are the input and the output terminals and the gate and the body contacts are used to apply bias voltage. Hence the output current flows between the source and the drain, and the gate is used to control this current flow, then the gate voltage is the basis of turning the transistor in ON state or in OFF state.

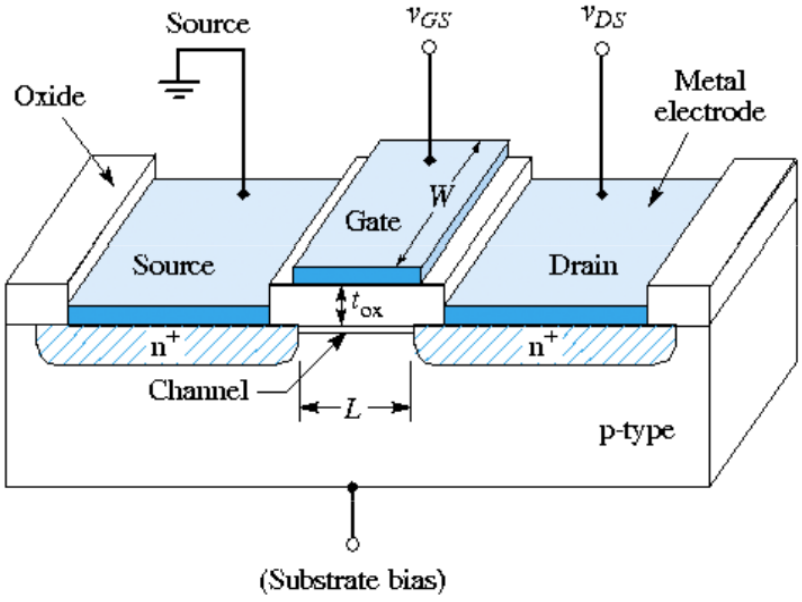


Figure 8: Schematic diagram of an n-cannel enhancement mode MOSFET [38]

The type of the charge carriers that assist in the source-drain current are used to classify the MOSFET. In an n-channel MOSFET the channel formation will be that of electrons while in case of a p-channel MOSFET it will be holes.

MOSFET can be classified on two other types as well based on their operation theory. These types are: Enhancement type and Depletion type MOSFET. Enhancement type is based on the channel formation only on the application of the gate voltage and hence is in OFF state when no voltage is applied, while in case of the depletion type MOSFET, the channel is already in formation and gate voltage is applied in order to turn the MOSFET to OFF state.

3.1 The Metal-Oxide-Semiconductor (MOS) Capacitor and Operation

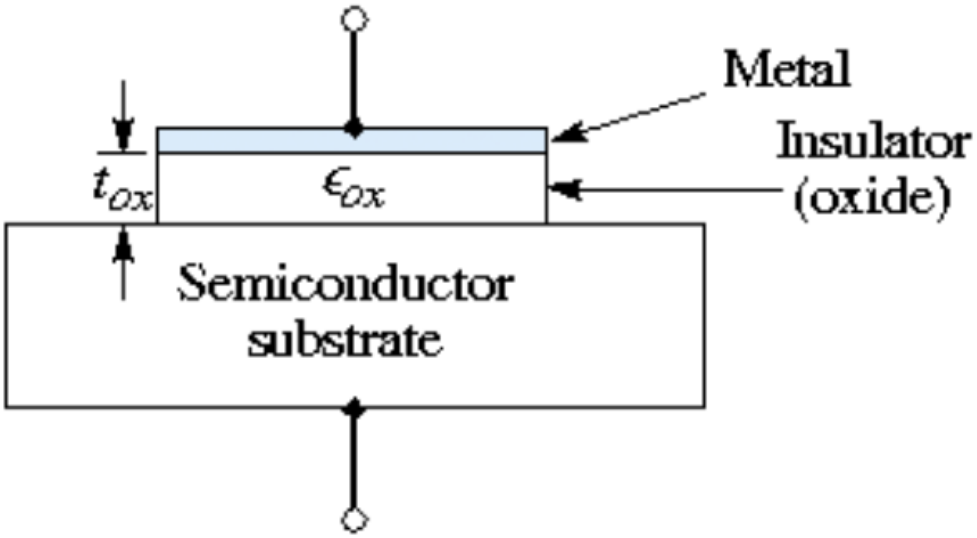


Figure 9: Basic MOS structure

An oxide layer is grown on top of a p/n-type semiconductor and a metal is placed on the oxide. The oxide layer provides isolation between the metal and the semiconductor. This was the structure of the MOS structure, which has changed a lot at present.

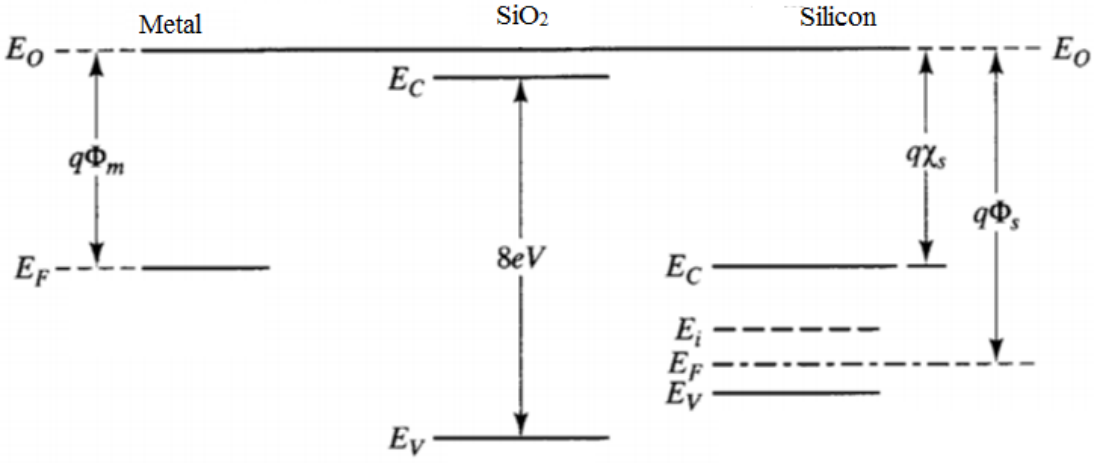


Figure 10: MOS band diagram before contact

In Fig. 10 we can see that the work function of the metal is less than that of the semiconductor. Hence, after the contact is made there will be charge transportation between the metal and the Silicon to as that the Fermi level of both gets aligned. This process will result in collection of electrons either at the metal interface or at the silicon interface depending on the work function of both. In the above specific case, as the work function of the metal is less, so the electrons will travel from the metal to the Silicon and a negative charge will collect at Si-SiO_2 interface.

An ideal MOS capacitor band diagram will look like Fig. 11, but since there is a difference in the work function, the actual band diagram will look like Fig. 12.

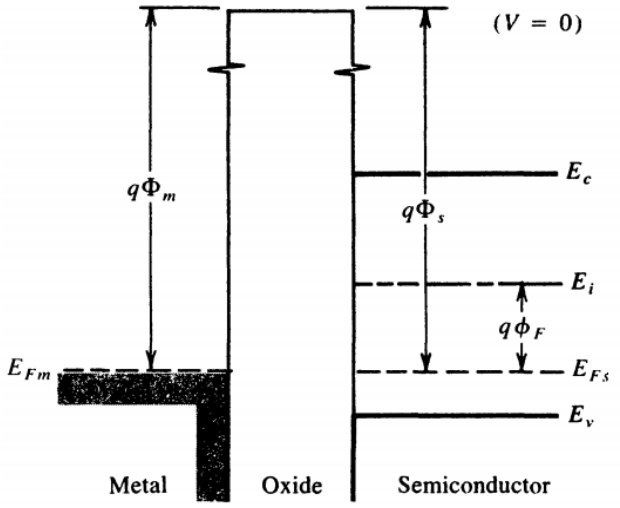


Figure 11: Energy Band Diagram for an ideal Metal Oxide Semiconductor structure at equilibrium [39]

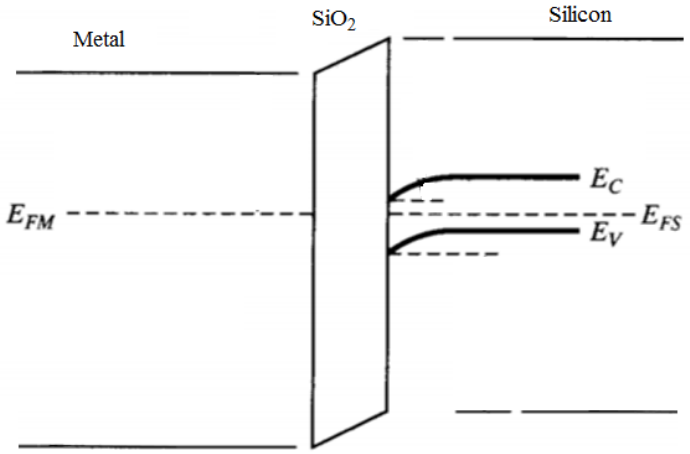


Figure 12: Band Diagram for MOS structure after contact

The Fig. 12 gives a band diagram in depletion mode, as there is a collection of electrons in the p-type semiconductor. The other cases are discussed further.

There are three cases possible:

- Accumulation Case
- Depletion Case
- Inversion Case

The Fermi levels of the metal and the semiconductors align themselves and there is no gradient. A potential barrier is formed between the metal and the semiconductor after the Fermi levels align. Due to difference in work function of the metal and the semiconductor, band bending occurs in the semiconductor.

Considering a specific case when the work function of the metal is less than the work function of the semiconductor and the semiconductor is of p-type we will obtain a depletion case. This happens because the work function of the metal is smaller than that of the silicon; electrons are transferred through the terminals of the device from the metal to the semiconductor. On the metal interface with the oxide, a thin sheet of surface positive charge is formed. On the semiconductor side, a voltage drop and an electric field are formed so that holes are driven away from the silicon adjacent to the surface of the oxide, leaving an excess of negatively charged ions. Therefore, the energy band in the semiconductor surface bends downwards.

The voltage drop across the insulator is a consequence of the charges stored on either side. Therefore a voltage needs to be applied to prevent this band bending. The Flat

Band Voltage is defined as the gate voltage applied to eliminate band bending at the surface of semiconductor and resulting in zero space charge in the region.

$$V_{FB} = \emptyset_M - \emptyset_S$$

$\emptyset_S$: Work function of semiconductor and $\emptyset_M$: work function of metal

If a bias voltage is applied further (after the application of V_{FB}), then following effects take place:

3.1.1 Accumulation Case

When there is an application of negative voltage on the metal contact side, the energy bands near the semiconductor surface are bent upward. The Fermi level in the semiconductor remains constant. As there is negative voltage applied, the electrostatic potential of the metal id reduced as compared to that of the semiconductor. This increases the energies of the electrons on the metal terminal compared to semiconductor. Therefore, E_{FM} the metal Fermi level changes and is then increased to a position qV above its equilibrium state, when a voltage V is applied. The metal acquires a negative charge on the surface with the oxide interface. Holes accumulate near the oxide semiconductor interface. Hence in case of p-type substrates, we have a p+ type region at oxide-semiconductor interface.

This change in the metal Fermi energy level relative to EFS, changes the oxide conduction band and introduces a tilt in it. This tile in the oxide is caused by the gradient due to the electric field.

$$E(x) = \frac{1}{y}\frac{dE_i}{dx}$$

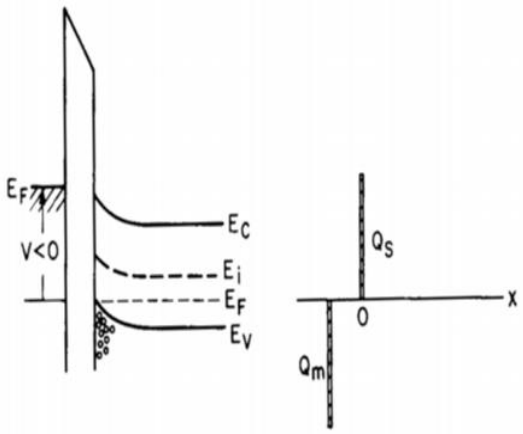


Figure 13: Accumulation Case in p-type

3.1.2 Depletion Case

The application of positive voltage increases the electrostatic potential of the metal thereby decreasing the Fermi level of the metal by the factor qV compared to its equilibrium position. Similar tilt of oxide energy band is observed as in accumulation case but the electric field direction is opposite this time. Bending of the semiconductor bands also takes place, and this time in the downward direction as there are electrons accumulating near oxide-semiconductor interface. So electrons are removed and the metal gets positively charged on the application of positive voltage. This positive charge attracts electrons on the semiconductor side. Due to the electron attraction, the holes in the p-type get depleted in the region near the surface, with ionized acceptors left behind. This case can be compared with a p-n junction system.

The hole concentration reduces in the depleted region, therefore E_i shifts nearer to E_F, and band bending occurs in downward direction near the semiconductor surface.

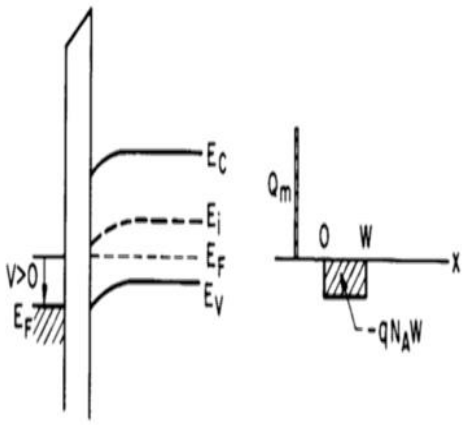


Figure 14: Depletion Case in p-type

3.1.3 Inversion Case

The effect seen in the depletion case will increase with the increase in the positive voltage applied. The bands will continue to bend more strongly, and at a sufficiently high voltage, the Fermi level will cross the E_i. In this case therefore, $E_F >> E_i$ means that there is a large concentration of negative charge near the conduction band and hence and n-type thin layer is formed because of the inversion phenomenon in a p-type material, since:

$$n_0 = n_i e^{(E_F - E_i)/kT}$$

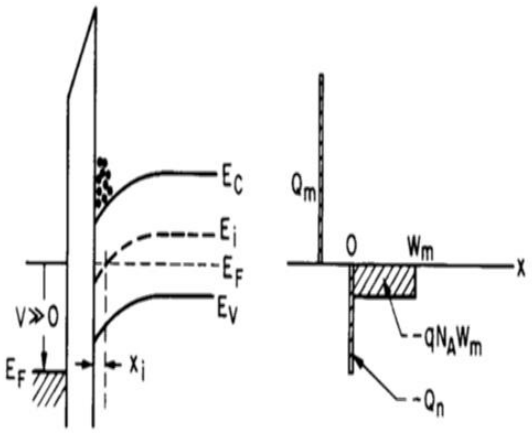


Figure 15: Inversion Case in p-type

The MOSFET operated according to the inversion case, where the band bending to so much that the bulk potential and the interface/surface potential are much different. The potential ψ is zero in the bulk semiconductor and ψ_s is the potential at the semiconductor surface, where ψ_B is Fermi potential.

$$q\Psi_B = E_i - E_F$$

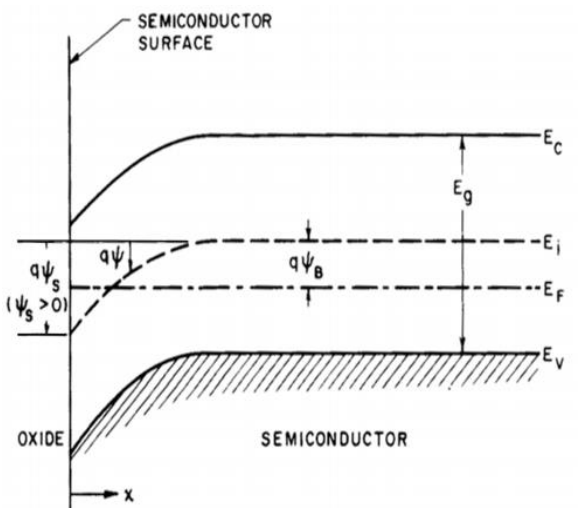


Figure 16: Analytical relation for surface and bulk potentials

$$\Psi_s(inv) \approx 2\Psi_B = \frac{2kT}{q}\ln\left[\frac{N_A}{n_i}\right]$$

kT/q= Thermal Voltage= V_T = 26 mV at room temperature (T= 300K)

N_A= Concentration of acceptor atoms

n_i= Intrinsic Carrier concentration =10^{10} cm^{-3} in silicon at room temp (T= 300K)

Hence we finally have (for p-type):

$\psi_s < 0$	Hole Accumulation (bands bend upward)
$\psi_s = 0$	Flat-band condition
$\psi_B > \psi_s > 0$	Hole Depletion (bands bend downward)
$\psi_s = \psi_B$	$n_S = n_P = n_i$ (intrinsic concentration)
$\psi_s > \psi_B$	Inversion (bands bend downward)

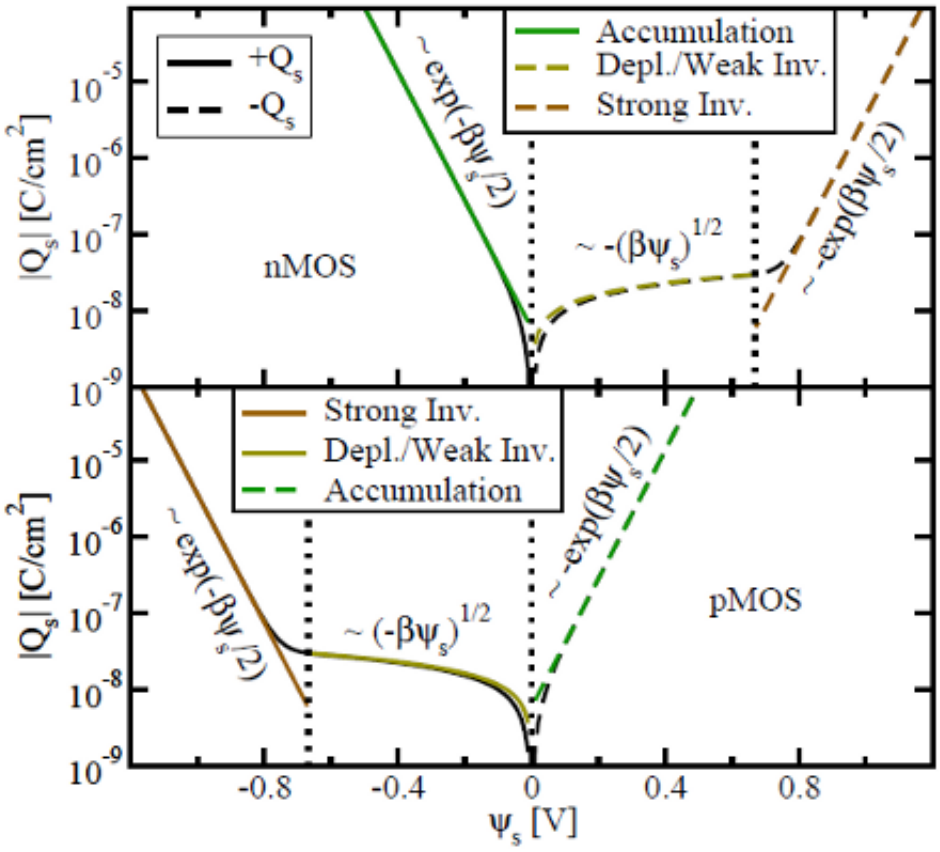


Figure 17: The surface charge density Q_S compared for both p-type and n-type semiconductors depending on. ψ_S. While the solid lines stand for positive Q_S, the dashed lines symbolize negative Q_S. [40]

3.2 MOSFET Operation

A MOSFET is a voltage controlled switch, as the application of the gate voltage controls the current flow between the source and the drain. Consider a p-type substrate and two n-wells formed in it, hence making an n-channel MOSFET or NMOS.

The well formation takes place mainly by ion implantation method. For n-well electron rich impurities like Phosphorus and Arsenic are added. The gate dielectric is a high-k dielectric to isolate the gate contact and the channel and also to provide maximum electric field to create a channel. Currently dielectrics like hafnium silicate, zirconium silicate, hafnium dioxide and zirconium dioxide are used to provide good capacitance with lesser area coverage. At the boundary of a single MOSFET we have field oxide that is used to isolate and provide reducing in electrical interference.

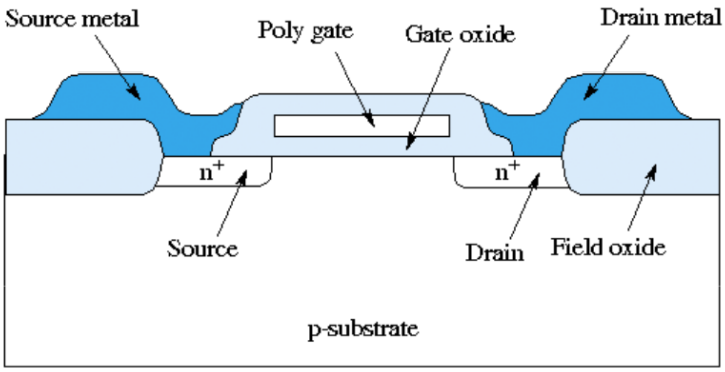


Figure 18: Cross section view of an n-channel MOSFET, showing the field oxide and polysilicon gate [38]

When the voltage on the gate terminal is positive compared to the substrate (which is also grounded like the source contact, hence V_G or V_{GS}), positive charges then start to deposit on the gate contact terminal. The electrostatic force of these positive charges on the gate terminal induces negative charges in the channel below and also repels away the holes present. These induced charges are actually the channel formed between the source and the drain terminal. This charge introduction in the form of a channel is because of the inversion case, where the Fermi level at the interface crosses the intrinsic level hence we have the inversion condition:

$$\Psi_s(inv) \approx 2\Psi_B$$

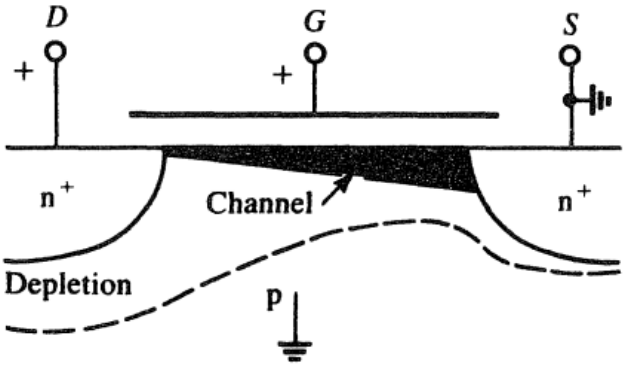


Figure 19: Channel formation in an NMOS with the application of gate voltage and drain voltage [39]

The function of the gate voltage is to induce the channel formation, but without the application of the drain voltage (V_D or V_{DS}, since source terminal is grounded) no current will flow between source and drain. Hence for a particular V_G the drain current (I_D) will increase with increase in the V_D, and the will saturate after a particular voltage. Therefore the function of the gate voltage is as a switch to allow the current to pass from source to drain.

3.3 MOSFET Characteristics

3.3.1 Output Characteristics

The plot between the drain current and the drain voltage with variable step values for gate voltage are called output characteristics. The linear region in the plot that starts from the origin is called the triode region and it is during the formation of this region that the current level at the drain terminal is increased. After a particular drain voltage the drain current saturates, and this point is called Pinch-off Voltage (V_{DSat}). Hence for the linear/ triode region we have:

$$V_G > V_{th} \text{ and } 0 < V_D < V_{DSat}$$

$$I_D = \frac{\mu_0 W C_{ox}}{L_{eff}} \left\{ (V_G - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right\}$$

Where,μ_0: Mobility,

W: Channel width

C_{ox}: Oxide (dielectric) capacitance

L_{eff}: Effective channel length

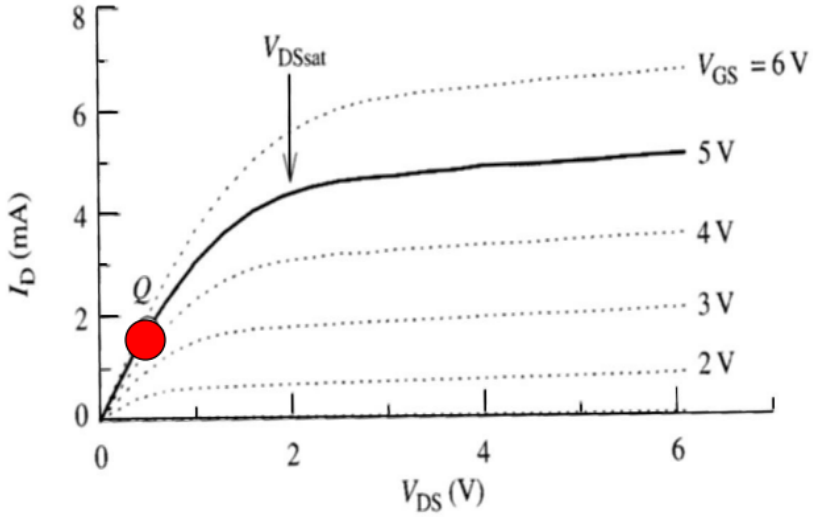


Figure 20: NMOS output characteristics for linear/ triode region

After the voltage is increased further than $V_{DSat,}$ the transistor goes into saturation region, where the effect of drain voltage on drain current is negligible and hence the current saturates. This is the ON regions of the transistor. Now at the pinch off point, the inversion region in the channel starts retracting away from the drain terminal because of the high drain voltage, now the vertical electric field that was holding the charges in the channel becomes horizontal and so the thickness of the channel at the drain terminal reduces greatly. Hence the channel now entered the saturation region.

$$V_G > V_{th} \text{ and } V_D > V_{DSat}$$

$$I_D = \frac{\mu_0 W C_{ox}}{2\, L_{eff}} \{V_G - V_{th}\}^2$$

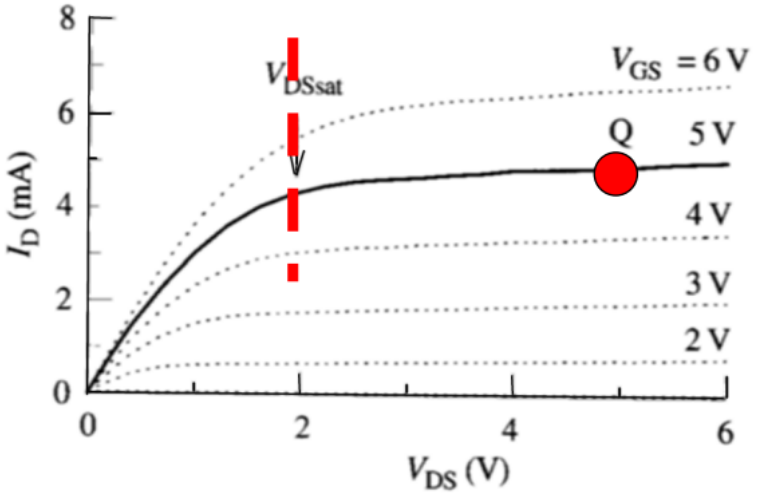


Figure 21: NMOS output characteristics for saturation region

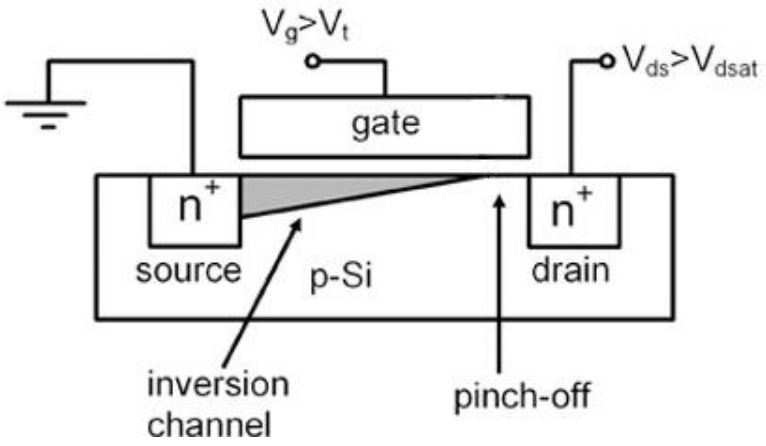


Figure 22: NMOS in saturation region showing Pinch-off region

3.3.2 Transfer Characteristics

For a MOS structure there is a particular gate voltage required to induce the formation of the channel. This minimum gate voltage is called the Threshold Voltage (V_{th}). Hence in order to have conduction, the gate voltage must be more positive than the threshold voltage for an NMOS and more negative than the threshold voltage for a PMOS. With the application of these voltages, the channel will be introduced and if there is a proper amount of drain voltage, the MOSFET will be said to be in ON state.

The transfer characteristics are the plot of drain current and the gate voltage at a particular drain voltage. These characteristics are most important to understand the device as we can extract a lot of parameters from the plot like mobility, on-off ratio, threshold voltage and sub-threshold swing voltage.

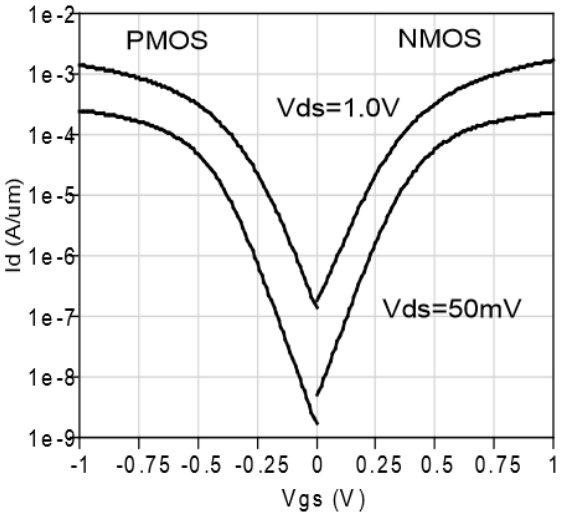


Figure 23: Transfer Characteristics of a 32 nm Intel PMOS and NMOS showing ~ 100mV/decade slope at V_{DS}=1.0V and 50mV [41]

- Threshold Voltage (V_{th}): It's if the most important parameter for a device, as it defines the voltage at which surface potential is double that of the body potential. The physical meaning of threshold voltage is that an electron channel with large electron concentration is formed on the surface of the semiconductor.

  $V_{GS}<V_{th}$, cut off mode

  $V_{GS}>V_{th}$, on-mode

  A positive effective gate voltage repels the holes from the silicon surface, leaving behind uncompensated negative acceptor ions. The charge is called depletion-layer charge.

  Density of the depletion charge: $Qd = qNaW$

  The effective voltage drop across the dielectric capacitor is:

  $$V_{GS} - V_{FB} - \psi_S = \frac{Q_d}{C_{ox}}$$ (For $V_{GS} < V_{th}$)

  At the threshold, $V_{GS}=V_{th}$ and $\psi_S = 2\,\psi_B$, therefore

  $$V_{th} = V_{FB} + 2\psi_B + \frac{Q_d}{C_{ox}}$$

- Mobility: It is an important factor while designing a device. It is the parameter that helps in differentiating between the devices and their capabilities. Mobility for devices based on Silicon is very high as compared to metal oxide based devices. The mobility measurement for a field effect device can be divided in two regions, first mobility for the linear region of the output characteristics and the other is the mobility for the saturation region. These can be calculated as follows:

  $$\mu_{lin} = \frac{L}{C_G W V_D}\left(\frac{\partial I_{Dlin}}{\partial V_G}\right)$$

  and

  $$\mu_{sat} = \frac{L}{C_G W}\left(\frac{\partial^2 I_{Dsat}}{\partial V_G^2}\right) = \frac{2L}{C_G W}\left(\frac{\partial \sqrt{I_{Dsat}}}{\partial V_G}\right)^2$$

  Hence the mobility values can be found out using these equations. So when we have $V_D < V_G - V_{th}$, the mobility data will correspond to linear mobility

and when $V_D \geq V_G - V_{th}$, then the mobility will be saturation mobility. If we plot $\sqrt{I_{Dsat}}$ with respect to V_G, we will get a straight line, in which the square of the slope will be proportional carrier mobility. If we extrapolate the linear part of the curve to intersect the Gate voltage axis, we will get the V_{th}.

- Subthreshold Swing (S): It is another important parameter that determines the performance of the field effect device. The value of subthreshold swig give the measure of how efficient is the channel formation with respect to the gate voltage. Hence it give the change in the drain current with respect to gate voltage. Higher the change in drain current for a given value of gate voltage the better the device is. It is the inverse of the slope of the transfer characteristic curve of the device and is measure in V/decade as its unit. The formula to determine subthreshold swing is:

$$S = \frac{\partial V_G}{\partial (log_{10} I_D)}$$

- ON/OFF Ratio: This is the last important measurement parameter for a device. The ON/OFF ratio as the name suggests, gives the ratio of the ON drain current and the OFF drain current. This is important because a higher ON/OFF ratio will ensure proper ON current while the device is switched ON and less leakage while the device is switched OFF. It is a unit less parameter and has a typical value of 10^6 for modern devices.

3.4 Comparison of a MOSFET and a Thin Film Transistor (TFT)

A TFT is also a Field Effect Transistor (FET) like MOSFET, but with some structural and operational differences. A TFT unlike a MOSFET is a layered planar structure.

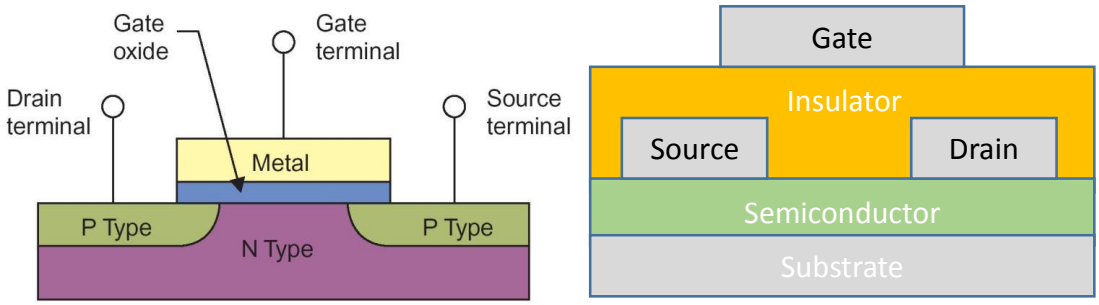


Figure 24: MOSFET (left) and TFT (right)

While in a MOSFET the source and drain are made by ion implantation of the dopant inside the substrate, where as in case of the TFT, the source and drain are made of metal and are directly used for contact terminals. In case of a MOSFET, the channel is formed in the substrate itself, but in a TFT, the substrate is just a support to fabricate the device. MOSFET is typically of the same structure as in the figure with source and drain in the same plane and then above them will be a dielectric and then a metal gate, but in case of a TFT the structure can vary a lot. Following are the possible structures possible in case of a TFT:

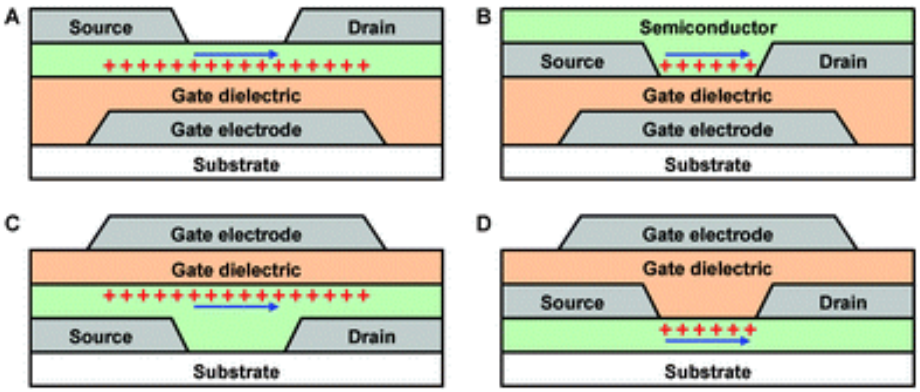


Figure 25: Different types of TFT structures [42]

- A: Bottom-gate (inverted) staggered TFT
- B: Bottom-gate (inverted) coplanar TFT
- C: Top-gate staggered TFT
- D: Top-gate coplanar TFT

The structure selected for an application depends mainly on the factors related to the purpose of the application and limitations due the fabrication process of the TFT to be made. For example, the Bottom-gate (inverted) staggered TFT is widely used for the fabrication of a-Si:H TFT, because of easy fabrication process and better electrical properties [43]. However, in case of the experiments performed in this thesis, the structure used is a Top-gate coplanar TFT, due to the metal used as source and drain contact i.e. Aluminium, which has melting point (933.47 K) close to the annealing temperature for the semiconductor used (773 K), hence it may result in destruction of the source and drain contact by the oxidation of the Aluminium.

Another difference is the use of the device, while a MOSFET is used mainly in a computing application and applications where high speed and performance is needed, a TFT is used for low cost applications where main concern is ease of fabrication, substrate flexibility and transparency, and the speed is not a concern like in display applications.

The working of the TFT is also a bit different compared to a MOSFET. A MOSFET while works when there is an inversion region formed in the channel, a TFT works upon the formation of accumulation region. Therefore for an NMOS-enhancement type MOSFET, a positive voltage would be applied to create a channel of n-type in a p-type semiconductor, while in a TFT positive voltage will be applied to create n+ type channel but in an already n type semiconductor. Although there are inversion case TFTs as well, but there are no accumulation case MOSFETs used.

Chapter 4: Experimental Procedure

The experimental design is such that it is done for two different types of structures, namely segmented device and the pixelated device. As the name suggests the pixelated device is much smaller than the segmented device. The purpose of both is the same but the application areas are different. The segment TFT design will be used to drive and control the large area OLED displays, whereas the pixelated device will be used to control small OLED displays.

The improvisation and optimization of the device is carried out with each layer of the TFT structure. In general, the semiconductor used is Zinc Tin Oxide (ZTO) with variable concentrations, the dielectric used in Poly (4-vinylphenol-co-methyl methacrylate) i.e. PVP-co-PMMA with some additives of poly(melamine-co-formaldehyde) i.e. PMF. The device characterization system used was 4200 Keithley Semiconductor Characterization System. TTP4 Cryogenic Probe Station by Desert Cryogenics was used for nano probing the devices for characterization. For the lithography processes, Karl Suss MJB4 Mask Aligner was used to make the source, drain and gate contacts.

In order to fabricate the two types of devices segmented and pixelated, the process was almost the same except the use of lithography for the pixelated device. Now, the next section will include the details about the device fabrication and processes. There are some common initial processes that are same for both the segmented and the pixelated device, like substrate cleaning and precursor preparation. These processes will be discussed initially and then the fabrication process for each of the type of TFT will be discussed individually.

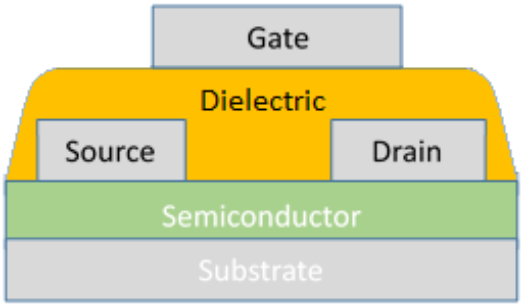


Figure 26: Final TFT device schematic

4.1 Substrate Preparation

The substrate preparation involves two steps: cleaning and activating the surface of the substrate (which in this case is Quartz). The cleaning of the substrate is very important. It involves a few processes to remove any dust or chemical adhering to the surface of the substrate. Hence, the process involves a mechanical procedure to remove dust and a chemical procedure to remove or dissolve any chemical impurity present.

The Quartz substrates were cleaned by submerging them in Acetone containment and sonicating the containment in ultrasonic bath for 15 minutes at room temperature. The purpose of the Acetone is to dissolve any chemical impurity and the ultrasonic treatment will rub away any dust particle attached on the substrate.

After this procedure, the samples were taken out and air gun (Nitrogen) was used to speed blow the acetone from the substrate. Thereafter the substrate is taken for UV-Ozonation.

The cleaning of the sample is done when the high energy UV light which is irradiated on the surface of the sample causing oxidation. This reaction is a photo sensitive oxidation which atomizes the Oxygen. So the UV is exposed on the heated substrate to start this reaction, making the surface hydrophilic and in return, volatile hydrocarbons come out as end product. UV-Ozonation is the process to activate the substrate surface by making it hydrophilic. This is done by exposing the heated surface of the substrate to UV radiations, which in air combine Oxygen atoms to form Ozone, which subsequently reacts chemical present on the surface to form water and get vaporized. Usually the temperature is set to be 150° C and the process is carried on for 20 minutes.

4.2 Semiconductor Precursor Synthesis (ZTO)

For both the pixelated and the segmented devices, the semiconductor used was Zinc Tin Oxide (ZTO) with variations in the molar ionic concentration and annealing temperature.

ZTO is a wide band gap n-type semiconductor material with the chemical formula:

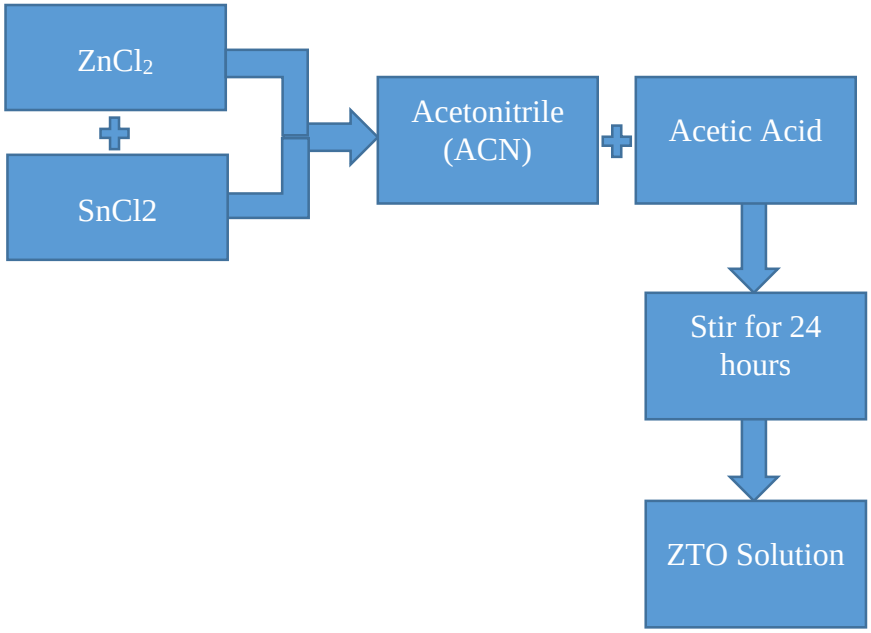
$$(ZnO)_x(SnO_2)_{1-x} \text{ , where } 0 < x < 1$$

There have been two types of structures of ZTO reported, trigonal ilmenite $ZnSnO_3$ and cubic spinel Zn_2SnO_4. Under atmospheric pressure, $ZnSnO_3$ exists in the ilmenite crystal structure which is known to exhibit excellent pyroelectric, dielectric, piezoelectric, and photostrictive properties. It has been observed that $ZnSnO_3$ slowly decomposes to Zn_2SnO_4 and SnO_2 at 873 K. Although Zn_2SnO_4 has a wide band gap of 3.35 eV but thin films of the same show a direct optical band gap ranging from 3.3 to 3.9 eV. Zinc Tin Oxide is a good choice for making oxide TFTs because they are highly stable and do not contain toxic, expensive and scarce elements like Indium and Gallium. It has good chemical stability with regards to oxidation and etching. Also it is physically robust and resistant to scratching and hence, forms a smooth thin film.

Table 2: ZTO recipes for different ionic molar concentrations

	ZnCl2	SnCl2	ACN	Acetic Acid
0.1 M	95.421 mg	67.689 mg	10 ml	0.5 ml
0.2 M	190.842 mg	135.378 mg	10 ml	1 ml
0.3 M	286.263 mg	203.067 mg	10 ml	1.5 ml
0.4 M	381.684 mg	270.756 mg	10 ml	2 ml

To prepare the ZTO solution (0.1M), 95.421 mg of $ZnCl_2$ and 67.689 mg of $SnCl_2$ were mixed and 10 ml of anhydrous Acetonitrile was added. To this solution 0.25 ml of Acetic acid was also added. The purpose of ACN is to act as a solvent for the solutes $ZnCl_2$ and $SnCl_2$, and the purpose of Acetic acid is to increase the solubility of the solution. This solution is stirred continuously using magnetic stirrer plates for 24 hours to ensure complete dissolution and homogeneity.



Flowchart 1: Semiconductor Precursor synthesis

4.3 Segmented TFT Device Fabrication Process

4.3.1 ZTO Spin coating

TFT fabrication is done on 1" x 1" Quartz wafer. For the segmented TFT, 0.2M ionic concentration ZTO was used a semiconductor. The solution processing method used was spin coating, which was done at 5000 rpm for 30 seconds. Before dropping ZTO on the sample, a layer of ACN was coated on the sample. This was done in order to improve the wettability of the substrate so that the ZTO layer deposited is uniform. While spin coating ZTO, PVDF filters (0.45 nm) were used to drop the solution on the sample. After deposition of a single layer of 0.2 M ZTO on Quartz, the sample was heated at 423 K for 1-2 minutes. This helps in the evaporation of the solvent (ACN) and prepares the sample for a next layer of ZTO. After heating, the substrate is allowed to cool down and then the same spin coating of ZTO and heating procedure is done two more time (with no ACN layer for these two rounds). Hence a total of three layers of ZTO are deposited on the Quartz substrate. Thereafter the sample is kept for annealing at 773 K for 1 hour in air. The spin coated metal chloride thin films are converted to high-performance semiconducting metal oxides through a reaction between the metal chlorides and H_2O present in the ambient.

Reaction like these requires some kind of catalyst or energy source to break the chemical bonds, start the reaction and also assist the subsequent condensation and

densification reaction. The energy source that we use is either thermal energy, i.e., heat or UV rays. These energy sources perform the following functions:

- Induce cleavage of alkoxy groups
- Decompose organic residues, solvent molecules and residual alkoxy groups
- Activate metal and oxygen atoms to facilitate M–O–M network formation
- Facilitate the rearrangement of the M-O-M network
- Facilitate the densification of the M-O-M network

4.3.2 Source and Drain Electrode Deposition

To fabricate source and drain electrodes, Aluminium metal was used. To make the electrodes on the semiconductor later, thermal evaporation procedure was used with the help of hard masks. On each of the Quartz substrates, two TFTs were made, hence two source and two drain terminals were fabricated. The thickness of the S/D (Source/Drain) electrodes was restricted to less than 40 nm. This is done in order to make sure that the dielectric deposited after the S/D electrode is deposited uniformly. Two of the following cases can occur with different electrode thickness:

- Thickness < 40 nm: Proper and uniform dielectric deposition (a).
- Thickness > 40nm: Uneven dielectric thickness at the edges (b).

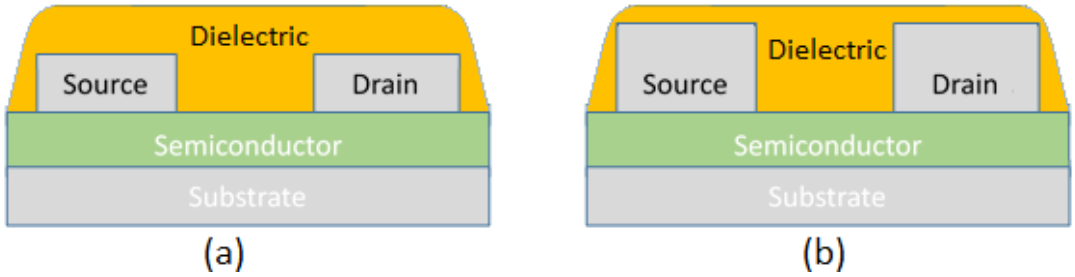


Figure 27: Effect of S/D electrode thickness on dielectric layer deposition

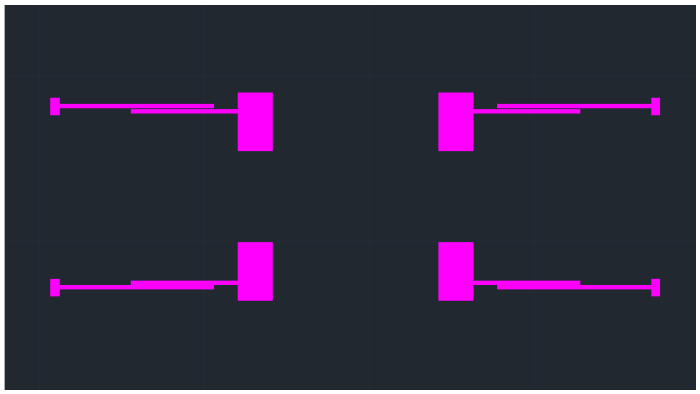


Figure 28: Source and drain mask with contact pads for terminal ends

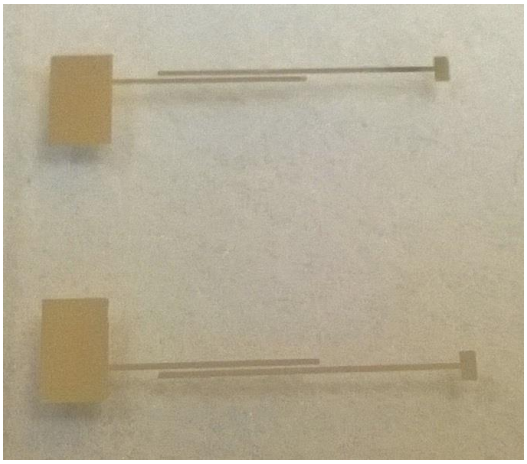


Figure 29: Metallized source and drain terminals with channel gap between them; below them is a ZTO layer

In the Fig. 29, four source and four drain terminals can be seen with a thin gap for channel formation present between them. The channel length and the width were 0.1 mm and 5 mm.

4.3.3 Dielectric Synthesis and Spin coating

The dielectric used for the segmented TFT device was PVP-co-PMMA polymer. It stands for Poly(4-vinylphenol-co-methyl methacrylate). To prepare the solution, a powdered mixture of PVP and PMMA polymers was used. The solution to dissolve this solute was Propylene glycol monomethyl ether acetate (PGMEA). To prepare the solution 1 gm of PVP-PMMA powder was dissolved in 9 gm of PGMEA liquid. The solution was stirred continuously for 24 hours to ensure proper uniformity in the solution.

Flowchart 2: Dielectric synthesis

To spin coat the dielectric, the solution was dropped on the sample using PVDF 0.45 nm filter and spun at 1000 rpm for 60 seconds. After this the sample was kept on the hot plate for annealing at 423 K for 1 hour. This annealing is necessary to enable crosslinking between the polymer molecules, which will help in reduction of the

leakage current through the gate dielectric. More the crosslinking better will be insulation property and lesser leakage.

4.3.4 Gate Electrode Deposition

This deposition of gate metal which is the same as the source and drain electrodes i.e. Aluminium, is done by thermal evaporation method using hard mask. The structure of the gate electrode is such that it totally covers the source and the drain terminal length wise as well as width wise. This will enable a proper electric field induction across the channel. The thickness of the gate electrode is kept higher than the source and the drain electrodes to ensure proper conduction.

For source, drain and the gate electrodes, Aluminium was used instead of Gold or Silver for the workfunction alignment. Aluminium has workfunction of 4.08 eV and Gold is 5.1 eV, so aluminium is better for n-type materials.

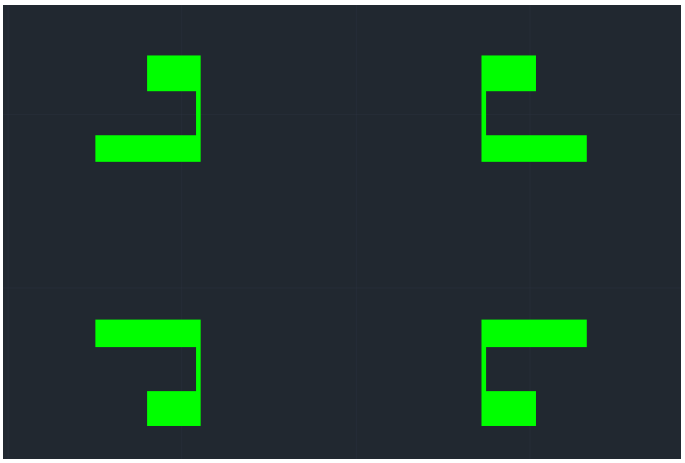


Figure 30: Gate mask with contact pad at the terminal end

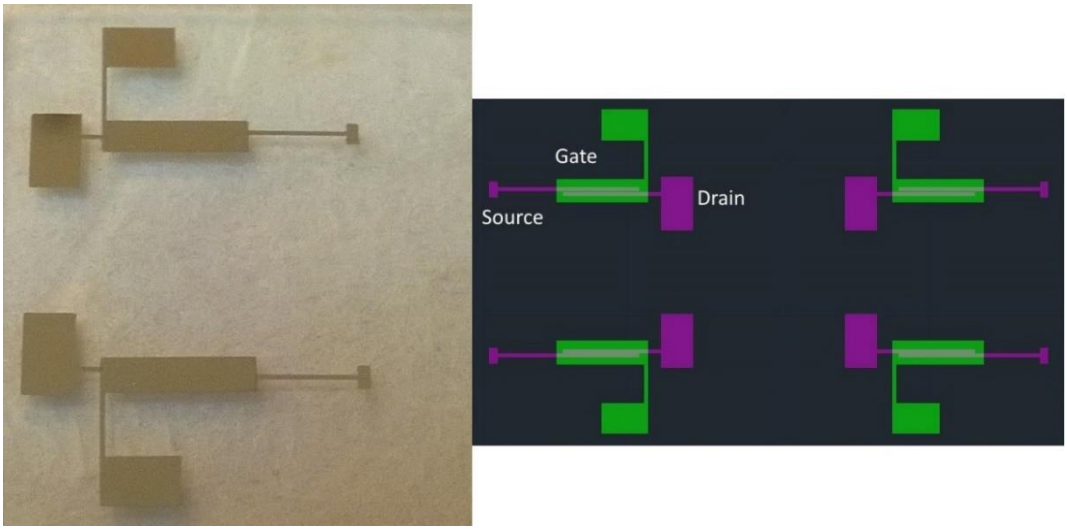


Figure 31: Gate mask overlapped with the source and the drain mask

4.4 Pixelated TFT Device Fabrication Process

The pixelated TFT device fabrication gets more complex as it involves more processing steps to ensure better devices. One of the major process step included is the use of photolithography to make the source, drain and the gate electrodes. As the dimensions of the devices are smaller, conventional use of hard mask is not possible. Therefore, the use of photolithography helps in printing the image of the mask as a layer on the semiconductor/dielectric which is later removed after metal is deposited. The changes were done in all the layers of the device i.e. the semiconductor layer, source and drain electrodes, dielectric and the gate electrode. First of all the quartz substrates are cleaned in acetone container kept in ultrasonic bath for 15 minutes and then treated with UV-Ozone to increase the surface wettability.

4.4.1 ZTO Spin Coat

The process to spin coat the ZTO solution is almost the same as that done for the segmented device, with some minor differences. In this case the ZTO solution taken was 0.3 Molar ionic concentrations. The molar concentration of the ions were increased to get higher ON current, which was decreased when 0.2 M ZTO solution was used, possibly due to change in the chemical composition of the dielectric (hence change in the viscosity) and the use of photolithography.

0.3M ZTO solution was spin coated on cleaned Quartz substrate three times each at 5000 rpm for 30 seconds. Thereafter the substrate was annealed at 773 K for one hour in air to complete the reaction for forming ZTO layer.

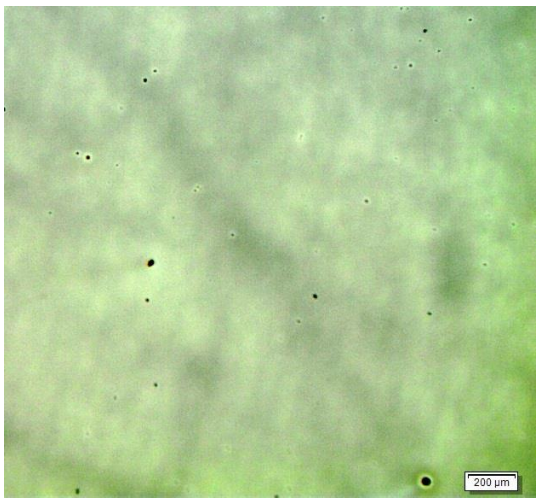


Figure 32: ZTO spin coated on Quartz wafer (some dust particles can be seen on the coating)

4.4.2 Photolithography for Source and Drain Electrode Formation

As the device features are very small, photolithography was used to define source and rain contact masks instead of using a hard mask. The equipment used for the photolithography was Karl Suss MJB4 Mask Aligner and the process was carried out in class 100 cleanroom. The wavelength used for the exposure was 405 nm UV light.

First of all the ZTO coated Quartz substrate was spin coated with a photoresist, which was AZ 5214 E Image Reversal Photoresist by MicroChemicals. It is a very commonly used positive photoresist and has a good adhesion to the surface. The photoresist was spin coated at 4000 rpm for 30 seconds, after which it was kept on hot plate preheated at 378 K for 60 seconds. This heating will help in the evaporation of the solvent of the photoresist and the film thickness will hence reduce to final 1.4 µm.

Table 3: Film thickness [µm] of photoresist AZ5214E as function of spin speed

Spin Speed (rpm)	2000	3000	4000	5000	6000
AZ 5214E	1.98	1.62	1.40	1.25	1.14

The sample is then places on the sample holder in the mask aligner, and the first exposure is done with the source and drain mask. The wavelength of the UV light used was 405 nm produced by a 350 watt Hg lamp with intensity 55 mW/cm^2. The UV exposure was done for 15 seconds. During this time, the exposed portion of the photoresist undergoes chemical reaction in presence of the UV light. Due to this the solubility of the exposed portion increases and that of unexposed portion remains the same.

After the 15 seconds of UV exposure, the sample is taken for development. During the development process, the sample is submerged in a chemical which dissolves the exposed portions of the photoresist, leaving a pattern made up of the unexposed photoresist. In the experiment, the chemical used for developing the photoresist AZ5214E after 15 seconds of UV exposure was AZ Developer (by MicroChemicals). The developer solution is prepared by mixing 1 part of AZ Developer with 2 parts of DI water. The sample is submerged in the developer solution made for 60 seconds, until all of the exposed photoresist gets dissolved.

This is a very important step, which will determine the pattern needed for the mask and also how much of the photoresist is still left over undissolved. Hence the time for how long the sample is submerged is important. After the sample is developed it is washed in DI water to remove any of the left over developer and the subsequently blow dried with Nitrogen gun. Finally the pattern of the mask is transferred to the sample.

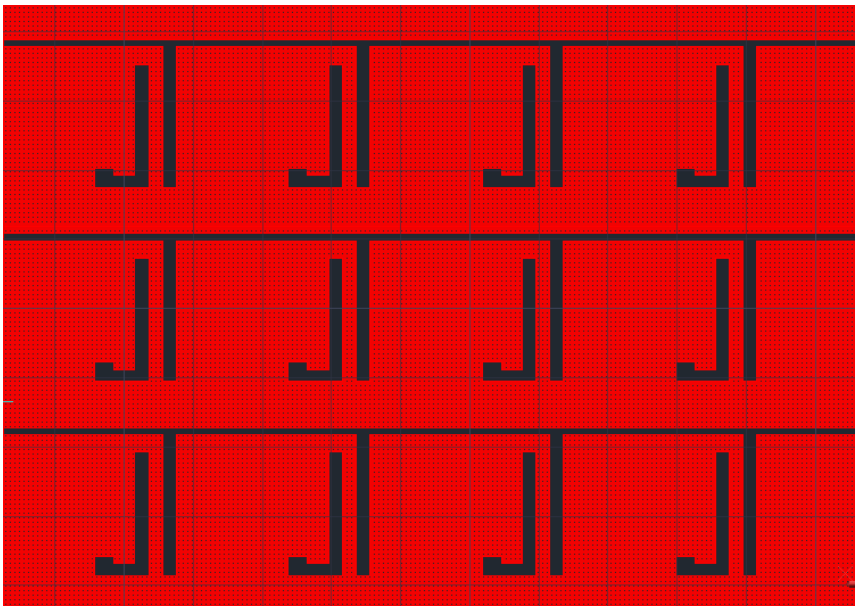


Figure 33: Photolithography mask for source and drain terminals with devices connected in series

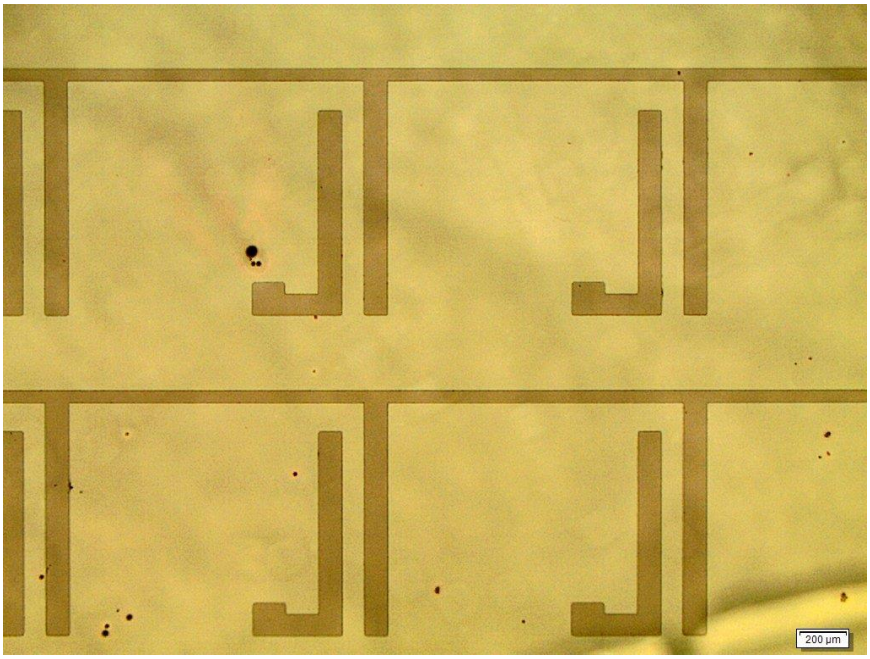


Figure 34: Source/rain mask formation after photolithography with ZTO coating below the photoresist layer (The design is the portion where there is no photoresist)

4.4.2 Source Drain Electrode Deposition

The next step in the process is to make the source and the drain using Aluminium by thermal evaporation method. The sample which already has a mask of the photoresist on it is place in the vacuum chamber of the thermal evaporator and aluminium is deposited with low deposition rate. Initially for the first 10 nm the rate of deposition is kept less than 0.1 Å/sec in order to introduce a good surface contact and to avoid any blister formation. This is very important in case of the pixelated device. After 10 nm the rate of evaporation can be increase to 1-3 Å/sec. In the case of the pixelated device as well we need to control the thickness of the Aluminium film deposited for the source and drain electrodes to less than 40 nm to ensure low leakage and better uniformity.

The metal deposition will be on the whole sample and so another process will be required after the deposition, which will involve removal of the unexposed photoresist, which will also remove the metal deposited over it, hence leaving the metal deposited on the pattern unharmed. The TFT devices are connected in series, with channel length and width as 100 µm and 890 µm.

4.4.3 Source and Drain Photoresist Removal

This process is done in order to dissolve and remove the unexposed portion of the photoresist. Hence the metal deposited on those specific portions will also be removed leaving behind a pattern of source and drain electrodes. This removal is done by putting the sample in Acetone and shaking it. Acetone dissolves the photoresists and the pattern is obtained. An additional process can be included to accelerate the removal of the photoresist, is sonicating the sample using ultrasonic bath. The sample can be submerged in Acetone and the sonicated. This accelerated the removal process. The process is done until the pattern is obtained and usually takes around 90 seconds.

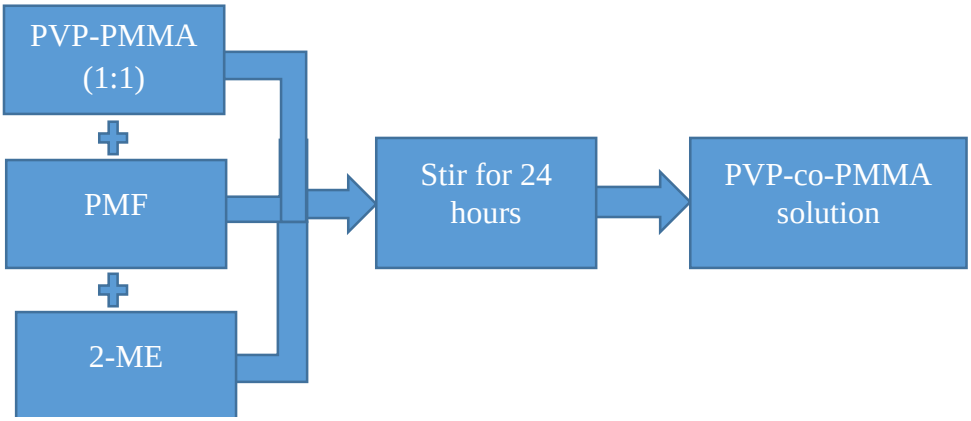
This removal process also depends on the thickness of the metal deposited. If the thickness of the metal is more, then it takes more time for acetone to penetrate the metal and dissolve the photoresist.

After the photoresist is all dissolved and the pattern is obtained, the samples is immediately blown dry using Nitrogen gun to remove the acetone.

4.4.4 Dielectric Synthesis and Spin Coat

After the source and drain electrode deposition, the dielectric is deposited over the sample. The recipe for the dielectric used is a bit different than the one used in segmented TFT device. The difference come because of the change in the solvent and addition of new cross linking agent to improve the adhesion, avoid acetone dissolvability and to reduce the gate leakage through the dielectric.

The recipe for the new dielectric used 1 gm PVP-co-PMMA with 1.38 gm PMF [poly(melamine-co-formaldehyde)] and dissolved in 8.5 ml of 2-ME (2-Methoxyethanol). The solution was stirred for 24 hours and then used as dielectric.



Flowchart 3: Dielectric Synthesis

PMF is the cross linking agent in this solution and also improves the adhesion. The spin coating of the dielectric is done by dropping the solution using a PVDF 0.45 nm filter and then spinning the sample at 1500 rpm for 60 seconds. The spin speed has been increase as compared to the one used for the segmented device. This is done because now as the recipe of the dielectric I different, the viscosity of the solution is higher and hence higher spin speed is needed to get a similar dielectric thickness.

After spin coating the sample is kept on the hot plate for annealing at 433 K for one hour. This will help in the formation of cross links between the polymers.

4.4.5 Photolithography for Gate Electrode Formation

This process will again need a photolithography step as a hard mask cannot be used for pixelated device. So the sample is coated with the photoresist AZ5214E again and spun at 4000 rpm for 30 seconds, heated at 378 K for 60 seconds, and then exposed with UV rays using a mask for gate patterning. Here as it is the second lithography step, there is a need of alignment of the gate pattern to exactly overlap the source drain electrodes. This is done using the same photolithography tool 'Mask aligner'. The channel of the TFT device is seen from the microscope and matched with the position of the to-be-deposited gate contact. The UV exposure is done for 15 seconds using 405 nm UV light produced by 350 watt Hg lamp, with intensity 55 mW/cm^2.

Now after the exposure the sample is taken for developing in the AZ Developer solution. A solution is prepared with 1 part AZ Developer and 2 parts DI water and the sample is dipped in the solution. The exposed part of the photoresist is dissolved and a pattern is formed. The sample is then washed in DI water and blow dried with Nitrogen gun.

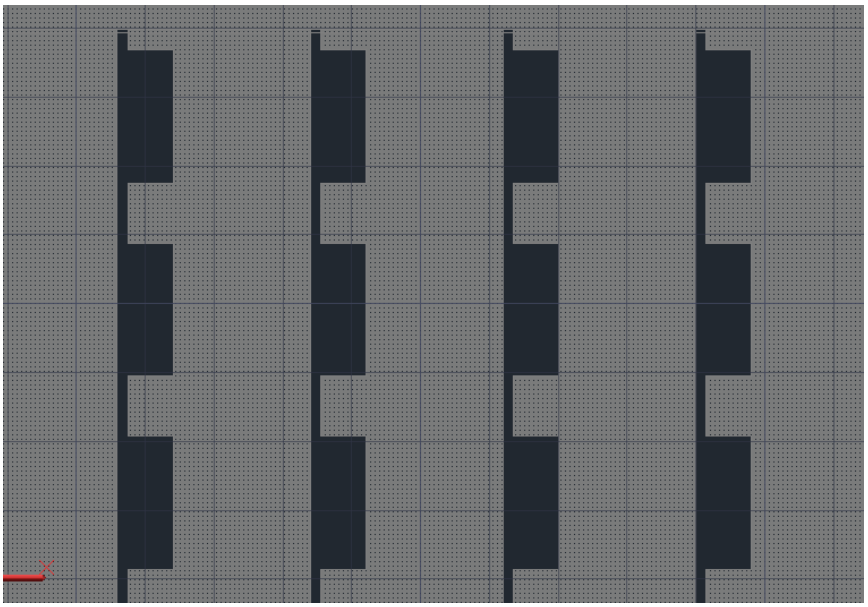


Figure 35: Photolithography mask for Gate formation connected in series

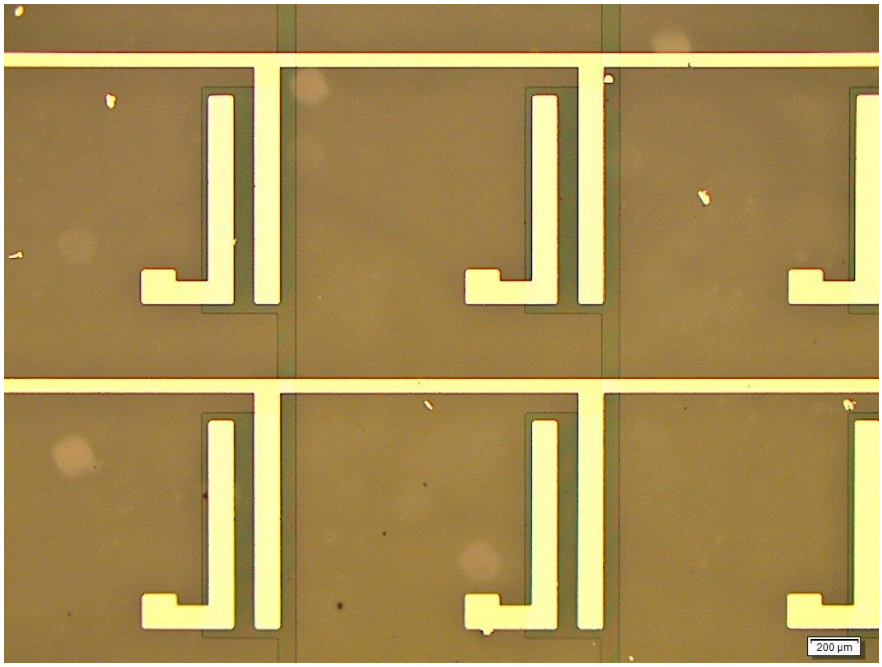


Figure 36: Metallized source/drain electrodes can be seen, with transparent dielectric above it, and then the gate mask formation after the photolithography process

4.4.6 Gate Electrode Deposition

To deposit the gate electrode, the sample is loaded in the thermal evaporator and the same process of Aluminium evaporation is done to deposit a layer of metal over the whole sample (with photoresist acting as a mask). The rate of evaporation is controlled exactly the way done for the source and drain electrodes for pixelated device.

4.4.7 Gate Photoresist Removal

The same process of removal of the unexposed photoresist is done as done for the source and drain photoresist removal. The sample is sonicated while submerged in acetone container for about 90 seconds. The acetone will dissolved the photoresist and remove the metal deposited over it leaving behind a gate pattern for the TFT device. The sample is the immediately blow dried with Nitrogen gun.

Note: In the dielectric recipe PMF was added for pixelated device. This addition was done in order to get a better cross linked dielectric. Now, if the chemical PMF was not added, then during the photoresist removal process, the dielectric will also be dissolve in the acetone, and the gate structure cannot be maintained. Hence addition of PMF assisted in better crosslinking thereby making the dielectric unable dissolvable in acetone and preserving the gate structure.

Finally a Pixelated TFT device is obtained.

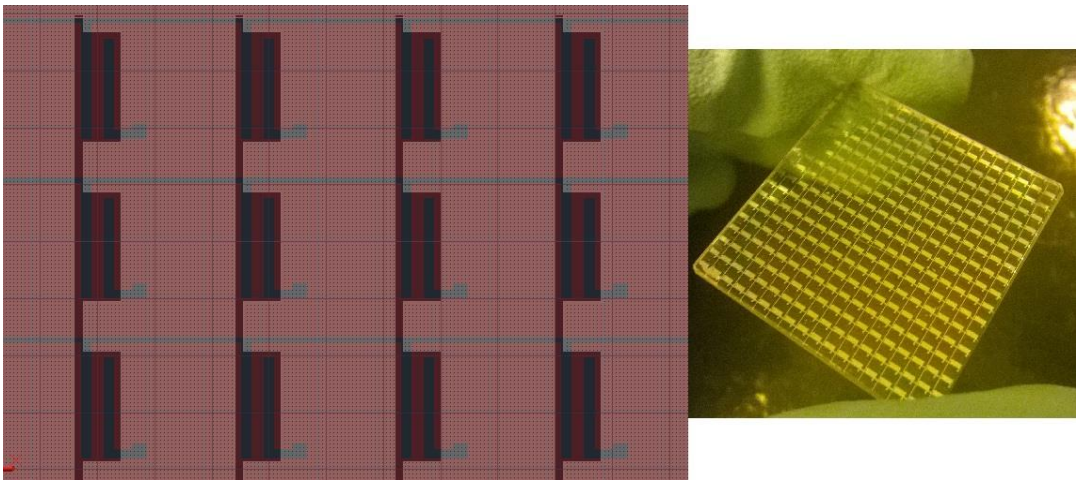


Figure 37: Overlap of Source/Drain and Gate masks

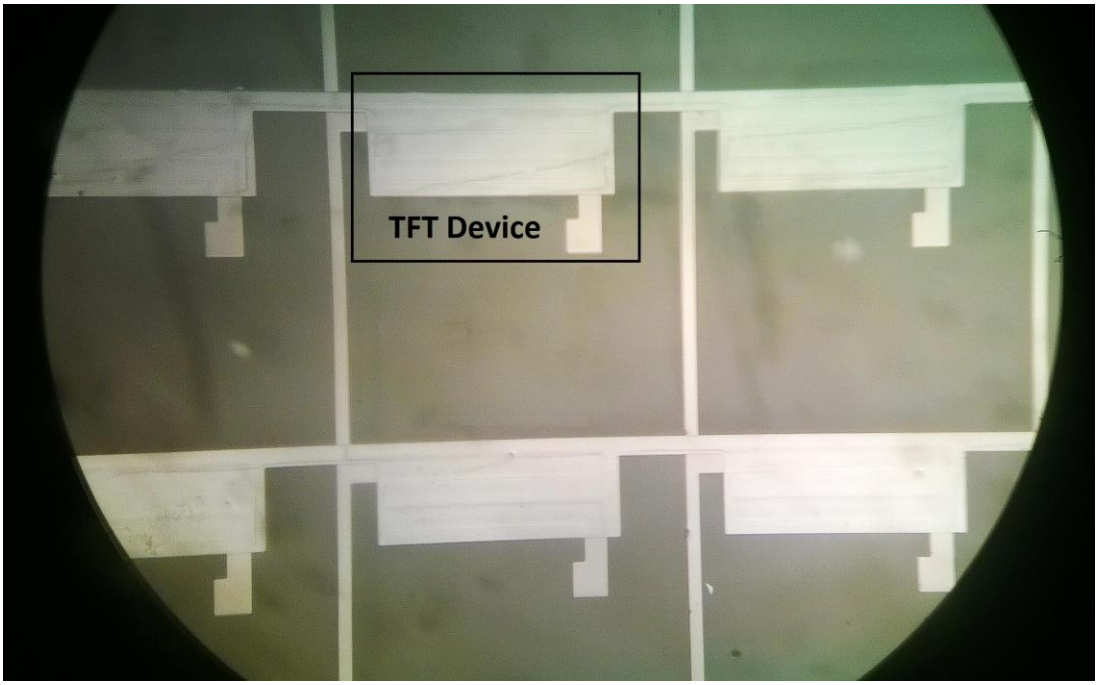


Figure 38: Final pixelated device with gate metallization above source and drain. The vertical metal strip connects all the drain electrodes and the horizontal strip connects all the gate electrodes

Chapter 5: Results and Analysis

5. 1 Segmented Device

5.1.1 Effect of Change in Ionic Concentration

For the segmented device, the ZTO ionic concentrations experimented with were 0.2M and 0.3M with Zinc to Tin ratio being 7:3 and the layer being amorphous in nature. As the channel width was quite large as compared to the pixelated device, the ON current was better for 0.2M and 0.3M ionic concentrations and there was no need for higher concentrations.

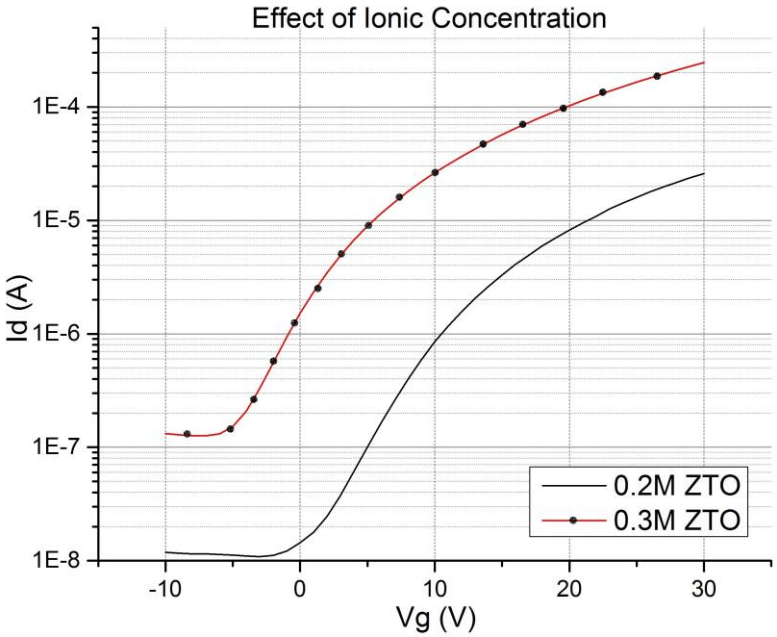


Figure 39: Transfer Characteristics (I_D-V_G) for 0.2M and 0.3M ionic concentration ZTO Segmented TFT

From the Fig. 39, it can be concluded that with increase in the ionic concentration of the semiconductor material the conductivity of the material increases. As it can be observed in the transfer plot that not only the ON current has increased, but the OFF current has also increased, which directly points out that the material has become more metallic in nature. 'More metallic' implies that there is an increase in the conductivity of the material in general regardless of the bias, so the ON and OFF current both will increase. This should be kept in mind while experimenting with the ionic concentration that although the ON current will increase, the OFF current will also increase and hence this type of modification or optimization is plausible only when there is sufficient margin for the OFF current.

5.1.2 Effect of Dielectric Spin Time

With the change in the dielectric spin time, the thickness of the dielectric is affected. This will change the leakage current through the dielectric and also the ON current as the thickness of the dielectric will affect the capacitance and which in turn will increase the ON current of the TFT.

$$I_D \propto C_{dielectric} \ and \ C_{dielectric} \propto \frac{\varepsilon}{d}$$

The spin times used in the experiment were 30 seconds and 60 seconds for the dielectric PVP-co-PMMA. From the plot in the Fig. 40, it can be seen that although there was a variation in the spin time, the gate leakage was almost the same in both the cases of about 11-13 µA. This can be explained by suggesting that the change in the spin time did not reduce the thickness of the dielectric to an extent which will increase the chances of charge penetration in the PVP-co-PMMA.

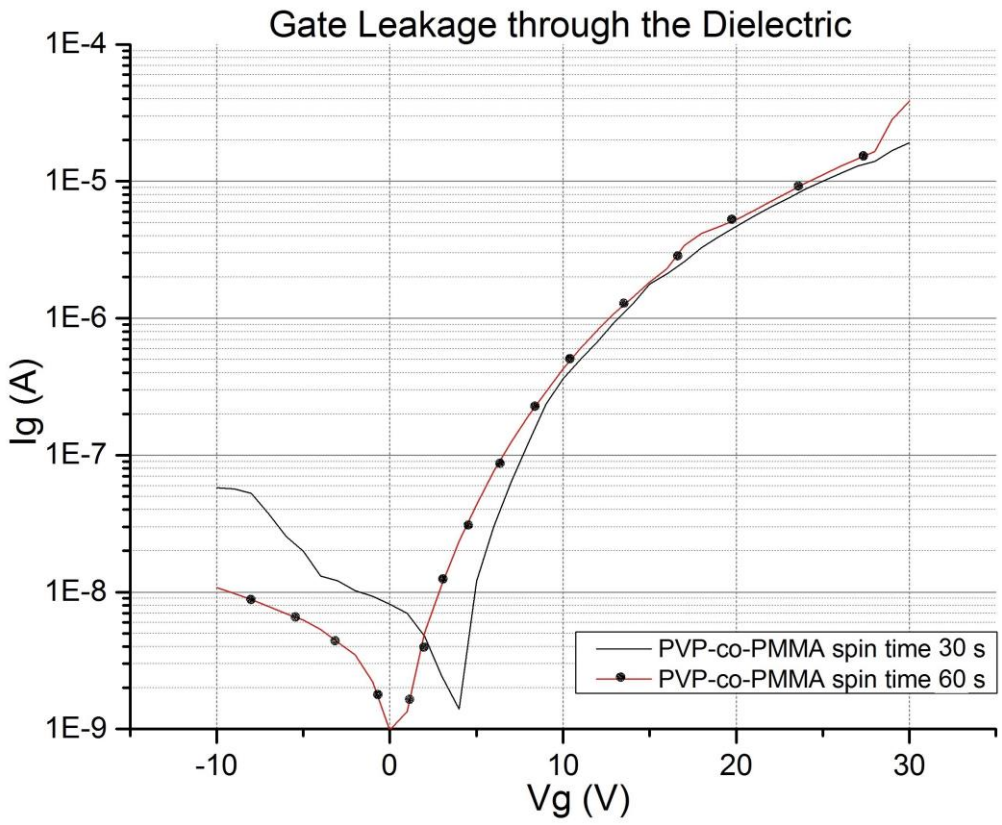


Figure 40: Gate Leakage through the dielectric with variation in dielectric spin time

Although when the transfer characteristics are compared for the two cases, the results give a difference in the ON current. For 30 second spin time, the dielectric layer would thicker as compared to the 60 second, and to the ON current should be higher in the case where the thickness is less i.e. for 60 seconds spin time. This can be seen from the plot shown below. Although the thickness did not decrease much, this can be linked with no big change in the leakage in the gate leakage plot in Fig. 41.

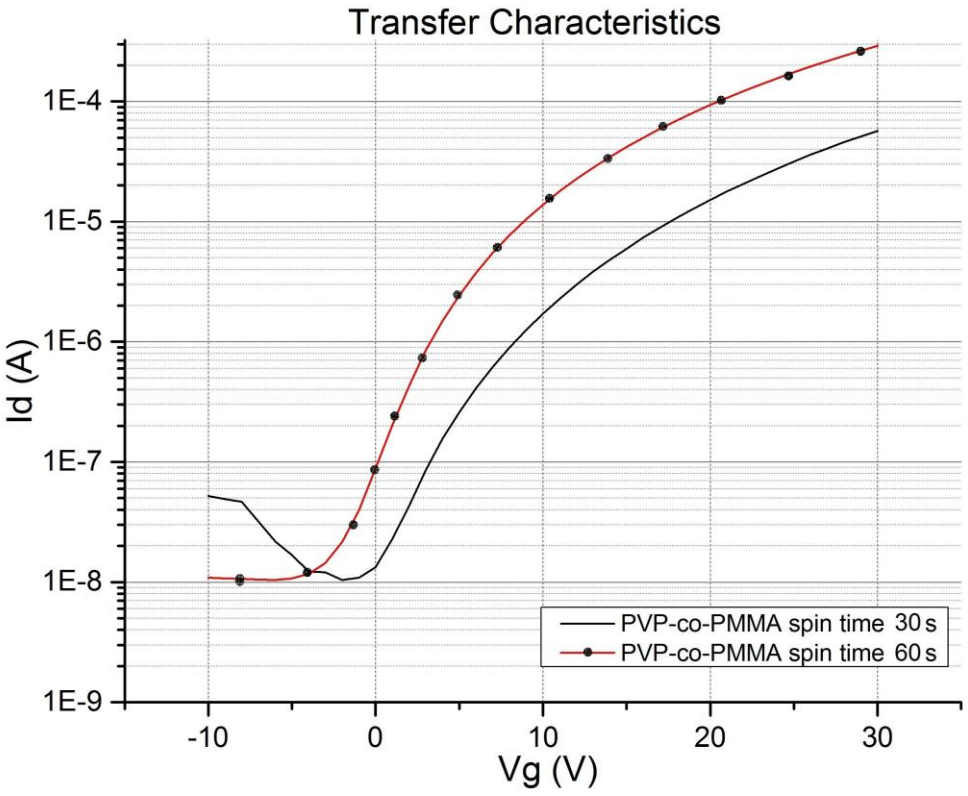


Figure 41: Transfer Characteristics (I_D-V_G) for 0.2M ionic concentration ZTO Segmented TFT with varying dielectric spin time

5.1.3 Final Optimized Device

For the final segmented device, the following process parameters were used and the device:

- Semiconductor: 3 layers of ZTO (0.2M) with Zinc: Tin::7: 3 spin coated at 5000 rpm for 30 sec.
- Annealing: ZTO annealing at 773 K for 60 minutes
- S/D Electrodes: 40 nm thick Aluminium source and rain electrodes
- Dielectric: PVP-co-PMMA spin coated at 1000 rpm for 60 seconds
- Annealing: Dielectric annealing at 423 K for 60 minutes
- Gate Electrode: Aluminium deposited using hard mask

These are the final segmented device process parameters which gave a good result with an ON current of more than 100 µA, OFF Current less than 100 nA. The gate leakage through the dielectric was also less than 10 µA. The gate leakage current depends on the nature of the dielectric material and the thickness of the material. High-k dielectrics will in general have lower leakage, and so will thicker dielectrics. The following curve is the plot of the final device that was used to switch OLED.

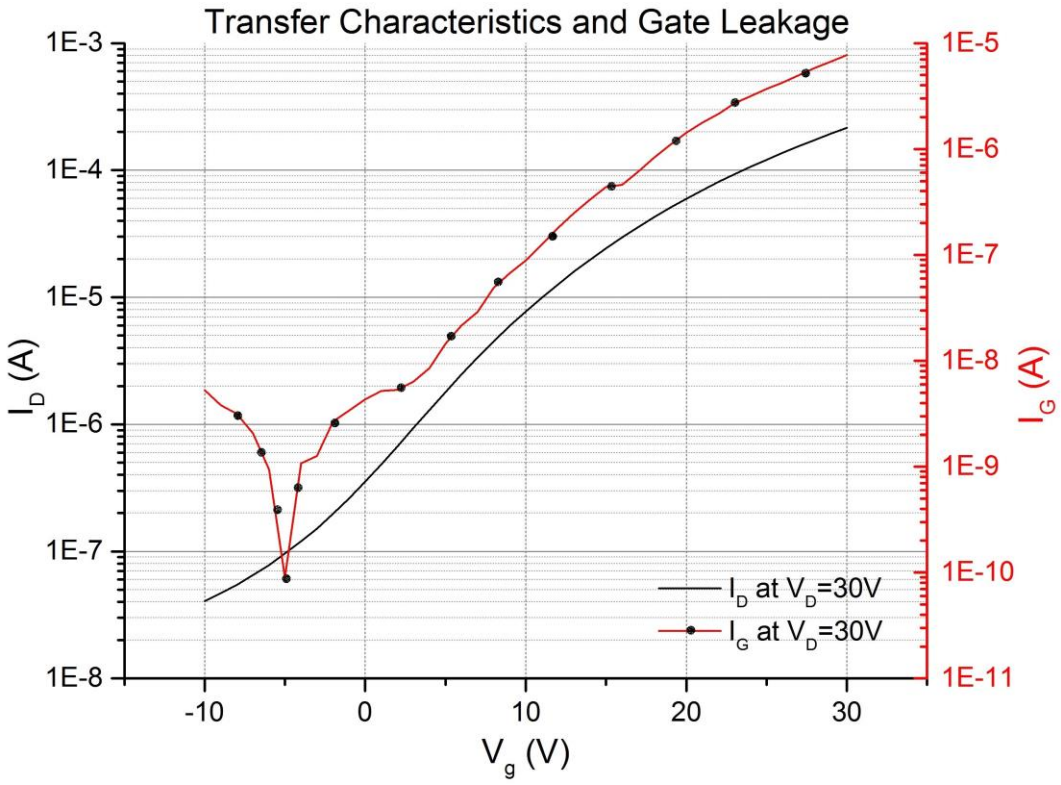


Figure 42: Final Device Transfer Characteristics (left black axis) with Gate leakage (right red axis)

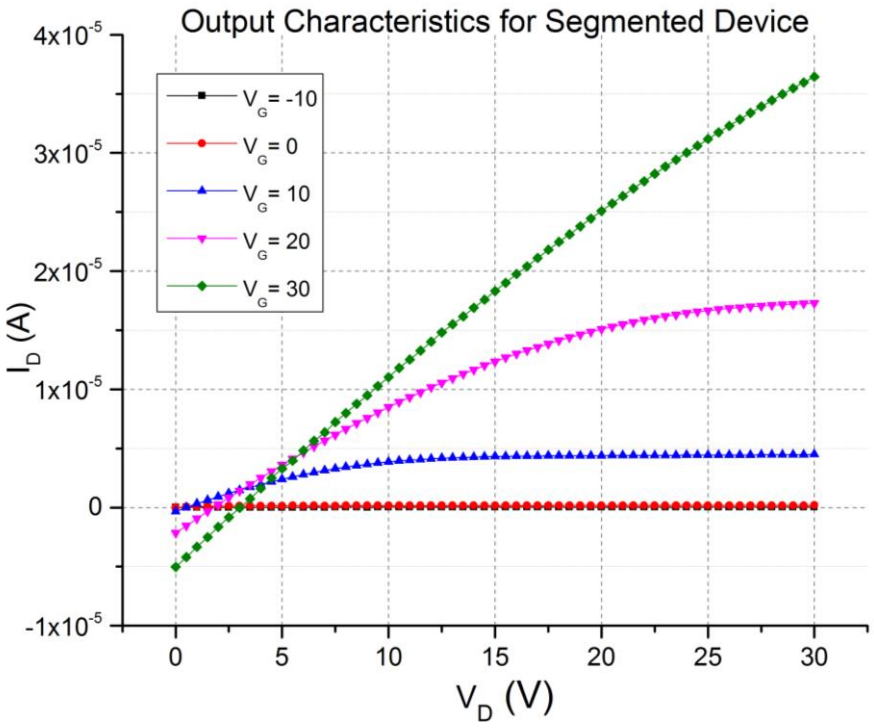


Figure 43: Output Characteristics for Segmented Device

The above plot depicts the output characteristics for the segmented TFT device. An observation can be made at the origin point of the graph, that the curves do not all start from zero. This is because of the leakage current in the device.

5.1.4 OLED Switching Using the Segmented Device

The TFT's drain terminal was connected to the OLED and a voltage of 30 V was applied continuously. The gate terminal of the TFT was supplied a square waveform of 0 V minima and +30 V maxima. This will create the switching ON and OFF action for the OLED.

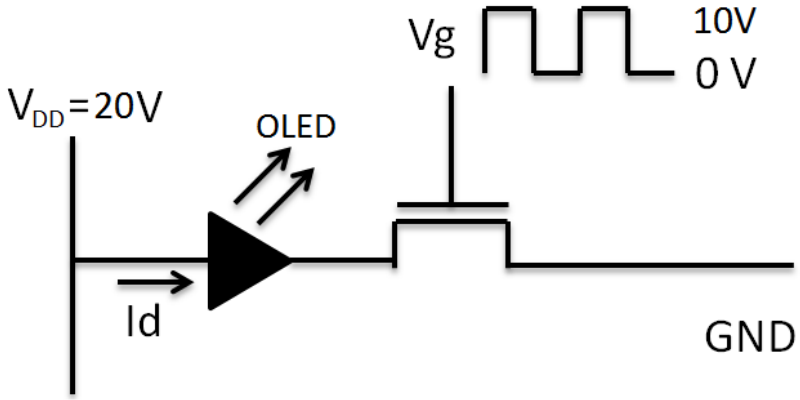


Figure 44: The OLED switching circuit diagram

The following is the device structure and the OLED deposition with the device which it will be driving. The OLED was deposited after the TFT fabrication was completed and the testing was done.

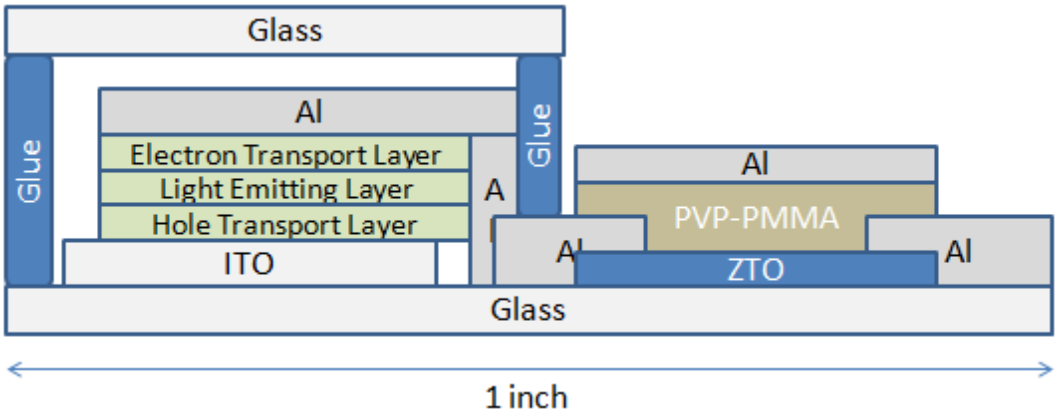


Figure 45: TFT device and the OLED structure schematic

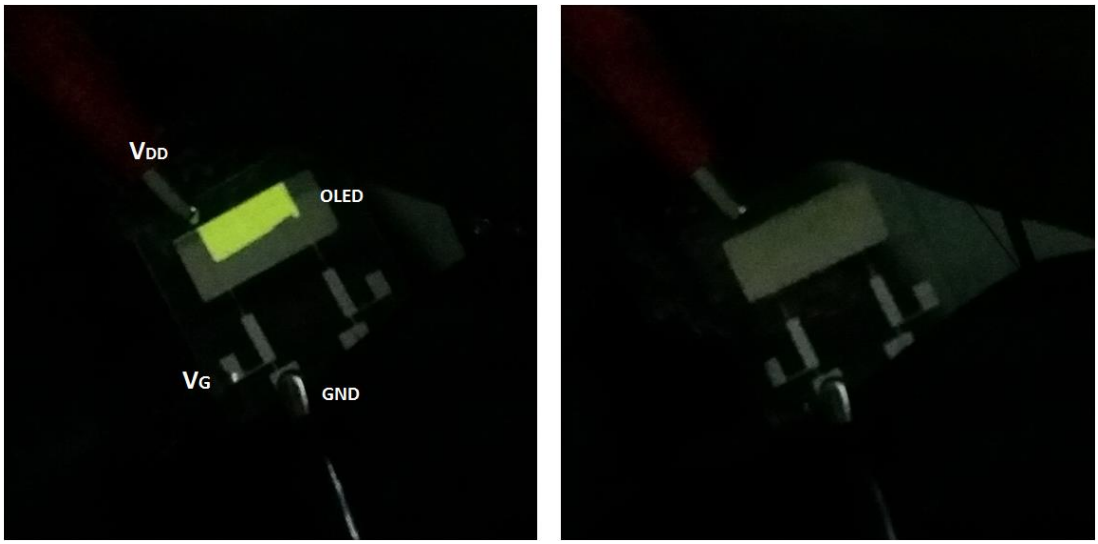


Figure 46: OLED switched ON (left) and switched OFF (right)

The Fig. 46 shows the picture taken of the OLED blinking action. The TFTs can be seen in the figure as well. The V_D applied was 20V and the Gate switching voltage applied was 9V. The area of the OLED device was 10mm x 5.5mm = 55 mm^2.

5.1.5 Segmented Thin Film Transistor Statistics

In order to freeze the fabrication process of a device, it is important to replicate the results using the exact same process. This is done in order to ensure that there are no glitches in the process and the device performance can be kept up to the mark even when fabricated in different locations with different equipment.

For the segmented devices, a total of 30 TFTs were fabricated in 2 different batches. Out of the total 30 devices, 22 devices showed good performance which give a yield of 73.33%. The device parameters like mobility, threshold voltage and ON/OFF ratio of each of these devices were calculated and then plotted to obtain statistical data for the fabrication process.

- Threshold Voltage

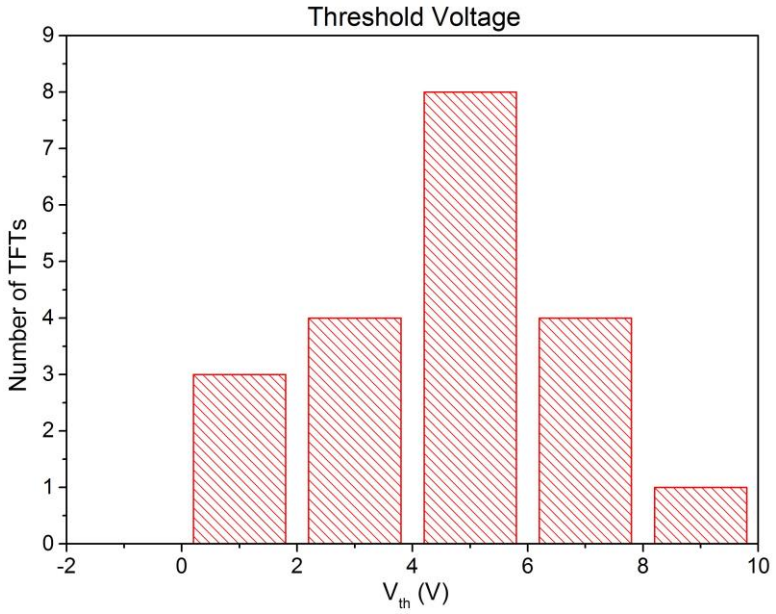


Figure 47: Threshold voltage distribution

For most of the devices the threshold voltage was found to be around 4V to 6V ±2V. Hence there is not much deviation in the threshold voltage which is good for the device fabrication process.

- ON/OFF Ratio:

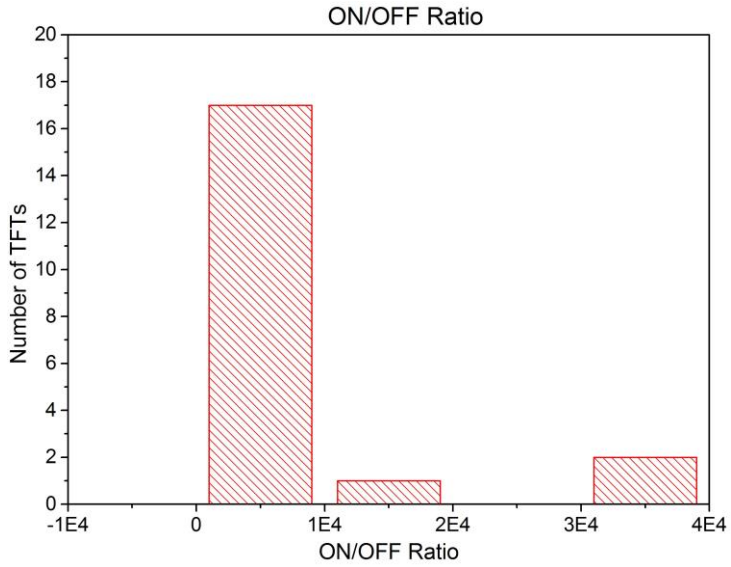


Figure 48: ON/OFF Ratio distribution

The ON/OFF ration of the devices is of the order 4. Hence when the ON current is about 100 µA, then the OFF current would be around 10-100 nA. This difference is sufficient for this specific application and it can be seen from the plot that most devices follow this trend.

- Mobility:

Similarly the mobility distribution shows the majority of the device with mobility of around 1-4 cm^2/V-s with occasional variation in the parameter.

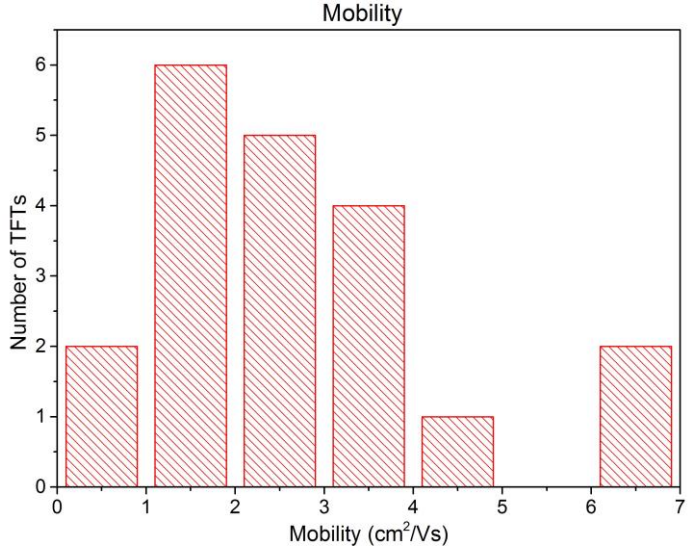


Figure 49: Mobility distribution

5.2 Pixelated Device

The results and the analysis of the pixelated device is broken up into several categories an explained in different sections. So the results are explained with respect to experiments on semiconductors and experiments on dielectric. Then there are further experimentations done within a category which are also explained after them.

5.2.1 Effect of Ionic Concentration

The change in ionic concentration of the ZTO solution will change the conductivity of the semiconductor. The 0.3M and 0.4M ionic concentrations with Zinc: Tin:: 7: 3 were experimented for pixelated TFT device. The deposited layer was amorphous in nature.

	ZnCl2	SnCl2	ACN	Acetic Acid
0.3 M	286.263 mg	203.067 mg	10 ml	1.5 ml
0.4 M	381.684 mg	270.756 mg	10 ml	2 ml

The spin coating of the both types of the solution was done exactly the same way, by consecutively coating ZTO, heating and cooling, and repeating this thrice at 5000 rpm for 30 seconds.

The addition of more solutes to increase the ionic concentration affected the performance in the following manner:

- It increased the ON current for the device
- It also increased the OFF current of the device.

This implies increasing the ionic concentration of the solution did not affect the semiconductor nature of the material, instead increased its conductive nature hence made it more metallic in nature. This type of alteration will be helpful only when high ON current is needed and the margin between the current OFF current and the desired OFF current is high. Therefore there will exist a trade off with the ON and the OFF current when modifying this parameter.

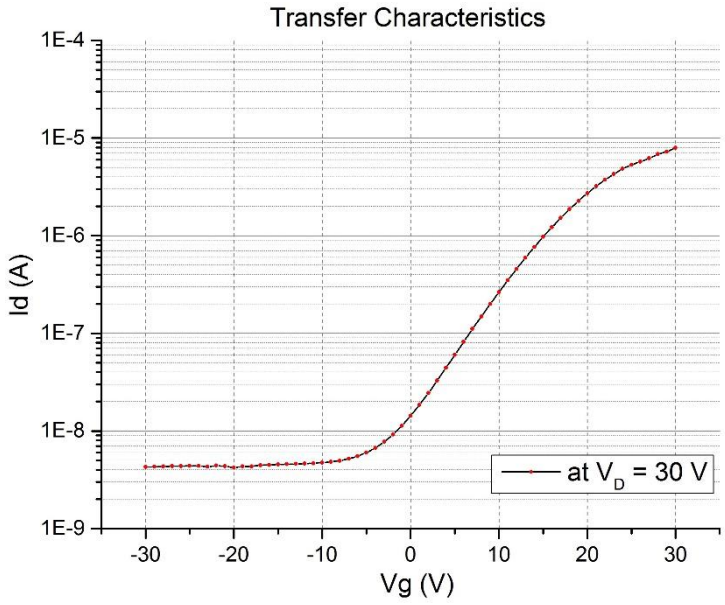


Figure 50: Transfer Characteristics (I_D-V_G) for 0.3M ionic concentration ZTO Pixelated TFT with W/L as 890/100 µm

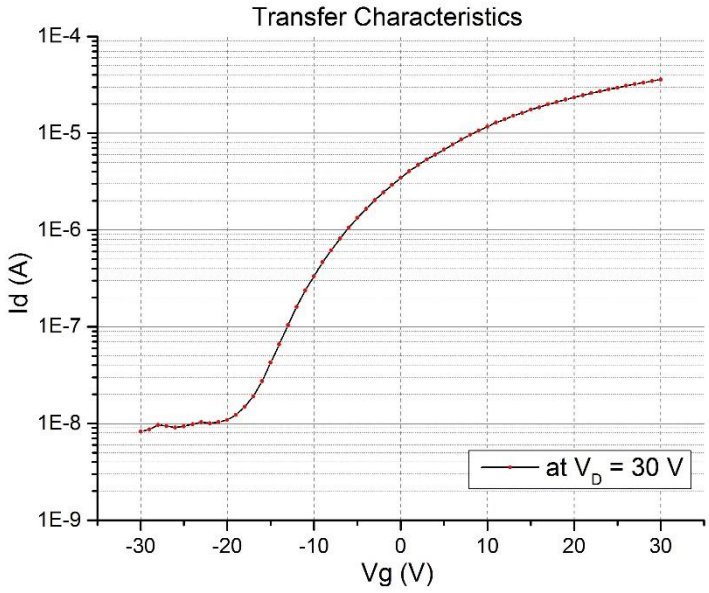


Figure 51: Transfer Characteristics (I_D-V_G) for 0.4M ionic concentration ZTO Pixelated TFT with W/L as 890/100 µm

For the 0.3M ZTO, the ON current was able to reach to 8 µA at 30V for both V_G and V_D, while the OFF current was about 4.2 nA. The specified OFF current to keep the TFT switched OFF was a maximum of 100 nA. Hence there was a huge room to increase the conductivity of the material, which will increase the ON current and also the OFF current. If the OFF current is below 100 nA, the OLED will work fine.

Therefore when the ionic concentration was increased to 0.4M, the ON current increased to 35 µA at 30V both V_G and V_D. Despite this increase, the OFF current was still under 100 nA and was recorded to be about 10 nA.

Following are the output characteristics of the same devices with 0.3M and 0.4M ionic concentrations of ZTO.

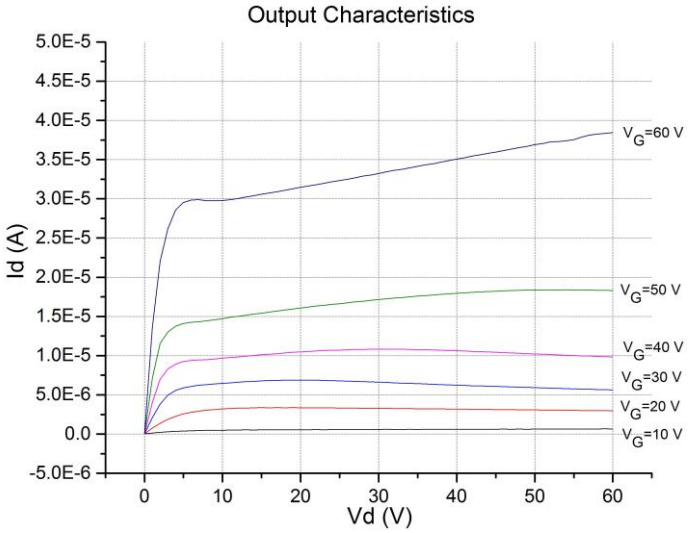


Figure 52: The output characteristics (I_D-V_D) for 0.3M ionic concentration ZTO Pixelated TFT with W/L as 890/100 µm

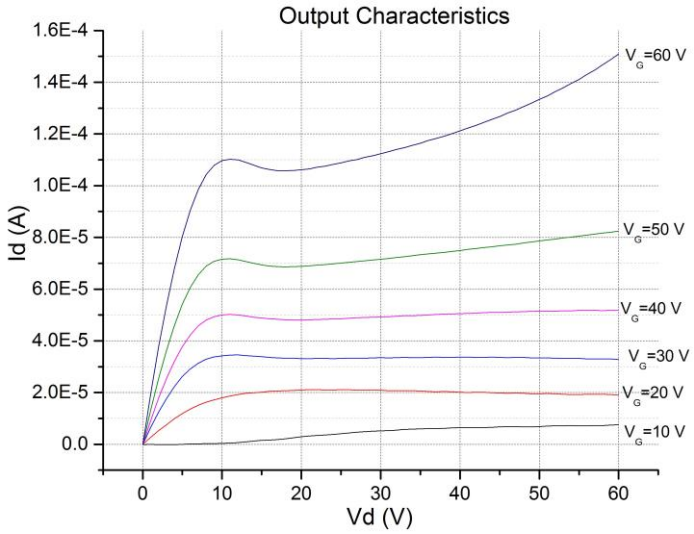


Figure 53: The output characteristics (I_D-V_D) for 0.4M ionic concentration ZTO Pixelated TFT with W/L as 890/100 µm

5.2.2 Effect of Dielectric Spin Speed

When the dielectric (PVP-co-PMMA + PMF) is spin coated the spin speed will change the thickness of the dielectric. The thickness of the dielectric is an important factor in determining the amount of electric field present in the channel because of gate voltage and the amount of leakage through the gate dielectric.

Lower spin speed:

- Thicker dielectric
- Lower electric field in the channel
- Low gate dielectric leakage

Higher spin speed:

- Thinner dielectric
- Higher electric field in the channel
- Higher gate dielectric leakage

Hence in order to get a high electric field in the channel and also low gate dielectric leakage, a trade-off is required to be made and an appropriate thickness is needed.

First set of experiments were carried out with spin speed of 1000 rpm for 60 seconds and then the second set had the parameters as 2000 rpm spin speed for 60 seconds.

For the first set of parameters, the thickness was higher, hence the leakage through the gate dielectric was less (< 1μA), while for the second set of parameters, when the dielectric was spun at double the spin speed of 2000 rpm, the thickness reduced, hence the leakage increased to about more than 10 μA.

This increase in spin speed was necessary in order to increase the effect of the gate voltage, and so this will increase the amount of electric field in the channel, leading to higher ON current. Higher ON current was achieved with thinning of the gate dielectric, but that also resulted in higher gate leakage.

This can be supported by the theory as well:

$$I_D \propto C_{dielectric} \ and \ C_{dielectric} \propto \frac{\varepsilon}{d}$$

Here we obtained a lower gate leakage with 1000 rpm.

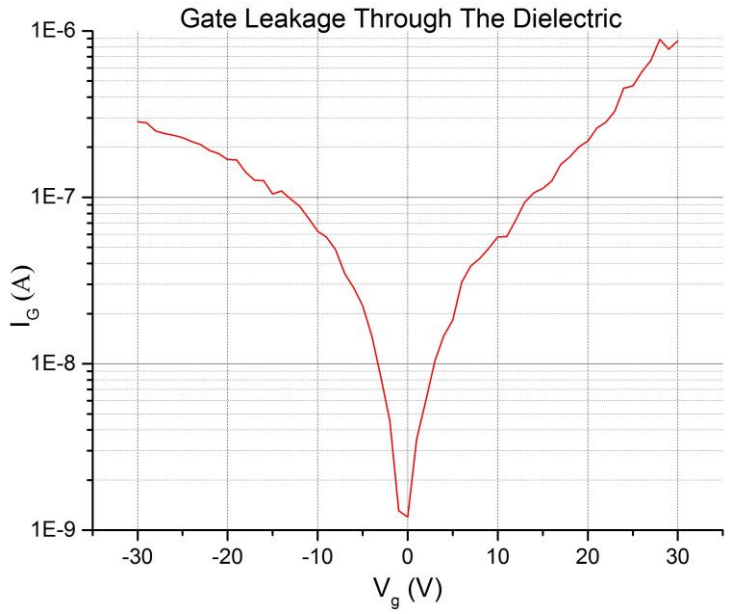


Figure 54: Gate dielectric leakage plot for PVP-co-PMMA + PMF dielectric spin coated at 1000 rpm for 60 seconds; gate leakage of 1μA at V_G=30V

For the second set of experiments (2000rpm), the gate leakage increased with reduced thickness.

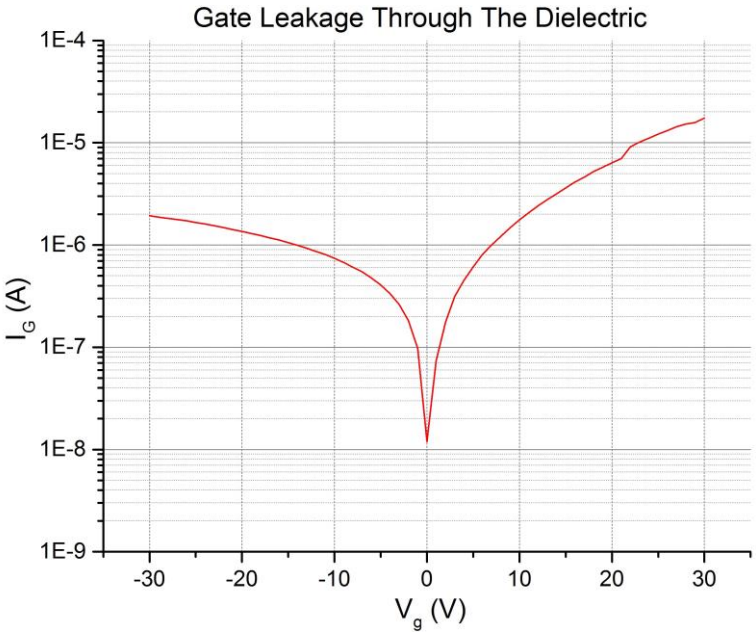


Figure 55: Gate dielectric leakage plot for PVP-co-PMMA + PMF dielectric spin coated at 2000 rpm for 60 seconds; gate leakage of 10.8 μA at V_G=30V

This is the transfer characteristic for TFT with dielectric spun at 1000 rpm, hence the ON current is comparatively lower (about 1 µA).

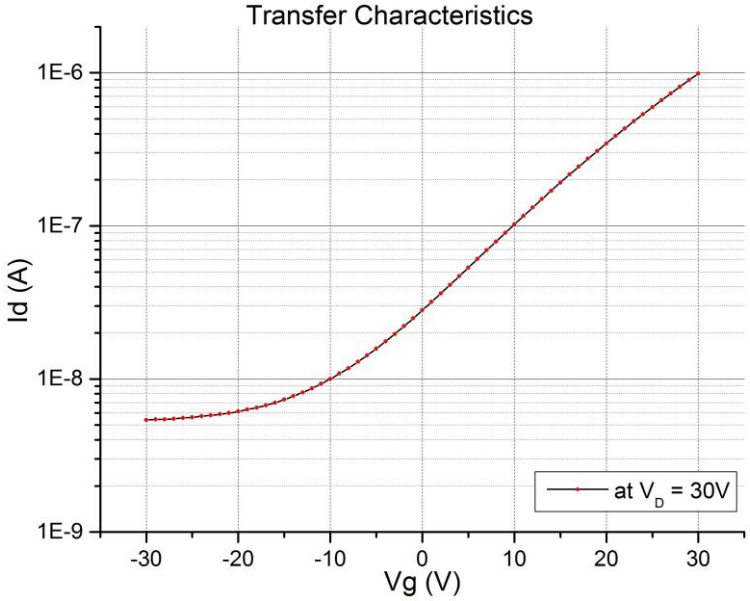


Figure 56: Transfer characteristics for PVP-co-PMMA + PMF dielectric spin coated TFT at 1000 rpm for 60 seconds; ON current of 1µA at V_G=30V

With higher spin speed of 2000 rpm, the ON current was increased to 12 µA, but at the cost of higher gate leakage.

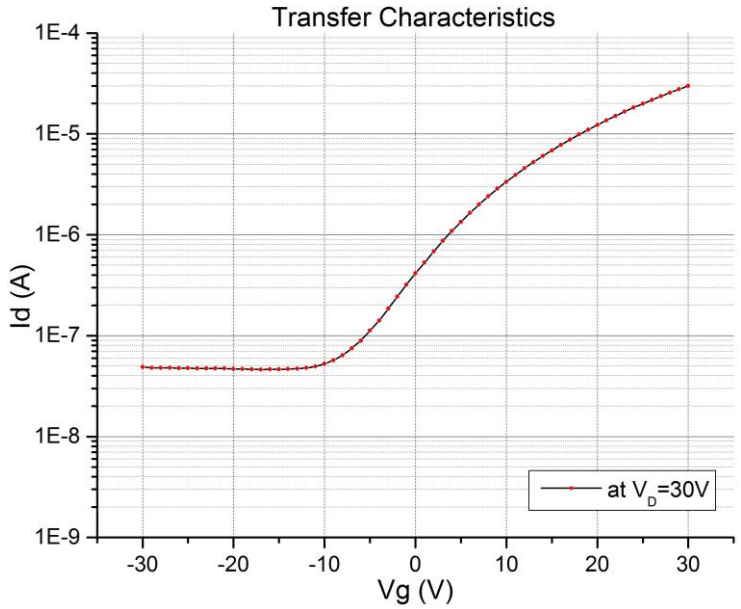


Figure 57: Transfer characteristics for PVP-co-PMMA +PMF dielectric spin coated TFT at 1000 rpm for 60 seconds; ON current of 12µA at V_G=30V

Hence a trade-off is required to balance the ON current versus the gate leakage.

5.2.3 Effect of Additive PMF to the Gate Dielectric

In the segmented device the dielectric used was PVP-co-PMMA. But for the pixelated device, an additive PMF was included in the PVP-co-PMMA solution as a cross linking agent. This was done in order to reduce the dissolvability of the dielectric in acetone while performing the lift-off for the photolithography for the gate electrode and also to reduce the leakage through the gate dielectric.

The experiment was done by varying the percentage of PMF in PVP-co-PMMA solution. The recipe for the dielectric used 1 gm PVP-co-PMMA with 1.15 gm PMF [poly(melamine-co-formaldehyde)] dissolved in 8.5 ml of 2-ME (2-Methoxyethanol). The solution was stirred for 24 hours and then used as dielectric. The dielectric was then spin coated using PVDF 0.45 nm filter at speed 1500 rpm for 60 seconds. The annealing was done at 423 K for 60 minutes and then the gate structure was deposited.

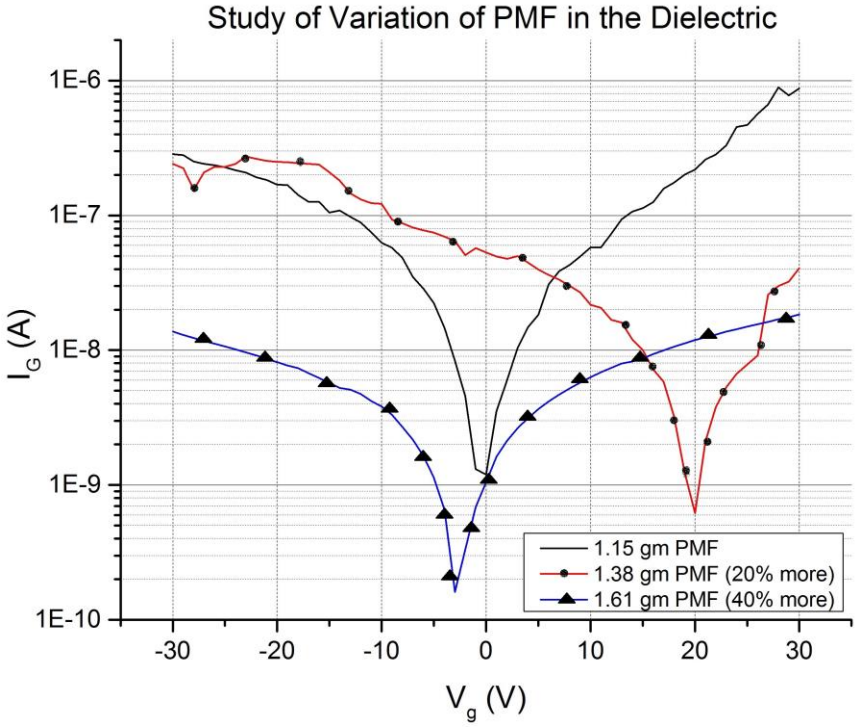


Figure 58: Study of variation of PMF percentage in the dielectric

With the addition of PMF, the viscosity of the solution changed and more PMF made the dielectric solution viscous and the thickness of the film increased with the addition of more and more PMF. So the reduction of gate leakage in this case is attributed to two factors i.e. the dielectric thickness and the amount of cross linking agent added. Another phenomenon that can be observed in the plots is the shifting of

the leakage plot for 1.38 gm PMF. This can be attributed to the presence of charge traps in the dielectric which shift the minima of the leakage curve to a value other than zero. So only then the internal traps are neutralized the current goes to zero.

Due to the change in the thickness, the ON current was again affected and therefore there was a need to select an optimum amount of PMF addition to the dielectric that can reduce the leakage substantially without affecting the ON current much. The trade-off was studied and concluded that the optimum amount of PMF addition would me 1.38 gm PMF to the dielectric since it reduces the leakage substantially (approximately by one order) and gives an ON current close to 1 µA.

What can be observed from the Fig. 59 is that 20% increase in PMF reduced the leakage by one order, but further increase in PMF to 40% did not increase the gate leakage by a big number. Similarly, if we observe the ON current for all the three cases, we can see that see that least amount of PMF addition gave better ON current since the dielectric thickness was less and more addition of the PMF decreased the ON current.

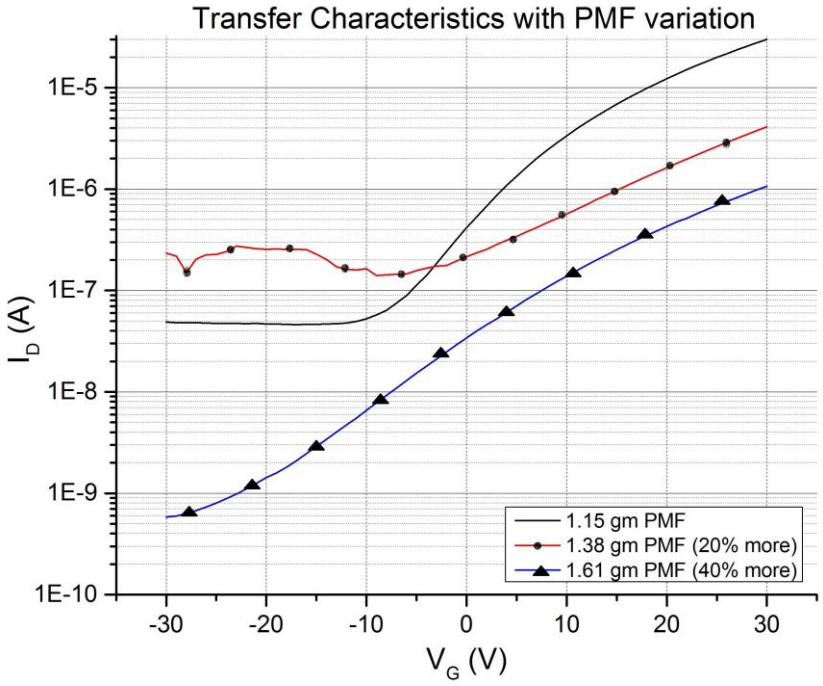


Figure 59: Transfer Characteristics for TFTs with variation on PMF percentage in the dielectric

Therefore for the final device, 1.38 gm PM was added to the PVP-co-PMMA solution for the dielectric solution. In order to increase the ON current more, the ionic concentration of the ZTO solution was increased from 0.3M to 0.4M for the final device.

5.2.4 Final Optimized Pixelated Device

The final optimized pixelated device involved a lot more process steps as compared to the segmented device. The following are the fabrication process steps for the pixelated device:

- Semiconductor: 3 layers of ZTO (0.4M) spin coated at 5000 rpm for 30 sec.
- Annealing: ZTO annealing at 773 K for 60 minutes
- Photolithography: Using source/drain mask, UV exposure on the 1.4 µm thick photoresist AZ5214E for 15 seconds and subsequent development
- S/D Electrodes: 40 nm thick Aluminium deposition on the whole substrate
- Lift-off: For source/drain formation, photoresist dissolved in acetone and lift-off is done
- Dielectric: PVP-co-PMMA+PMF spin coated at 1500 rpm for 60 seconds
- Annealing: Dielectric annealing at 423 K for 60 minutes
- Photolithography: Using gate mask, UV exposure on the 1.4 µm thick photoresist AZ5214E for 15 seconds and subsequent development
- Gate Electrode: Aluminium deposition by thermal evaporation on wafer
- Lift-off: For gate contact, photoresist dissolved in acetone and lift-off is done

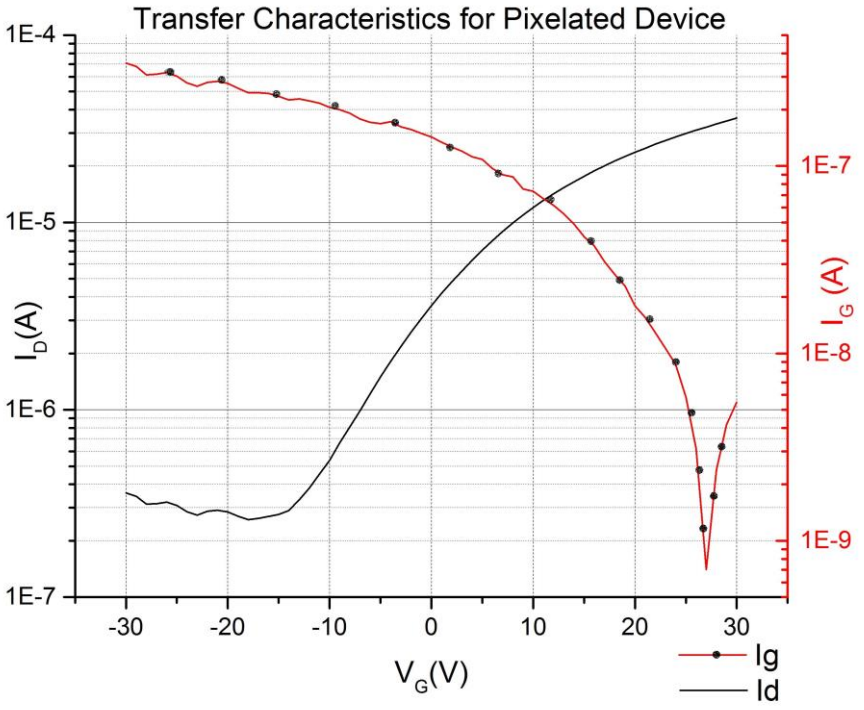


Figure 60: Final Transfer Characteristics of Pixelated Device

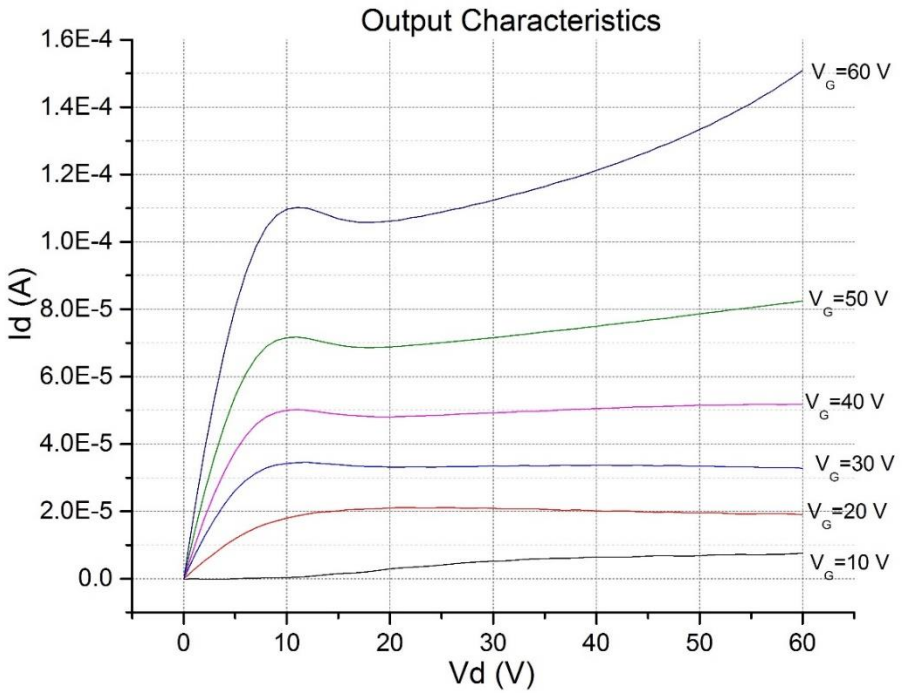


Figure 61: Final output characteristics (I_D-V_D) for pixelated device

For all these devices, forward and backward scanning for the gate voltage was conducted while electrical measurements made for the transfer characteristics. Due to use of dielectric PVP-co-PMMA, the trapping of the charges was minimized. Below is the plot for the transfer curve forward and backward trace and least amount of hysteresis is seen.

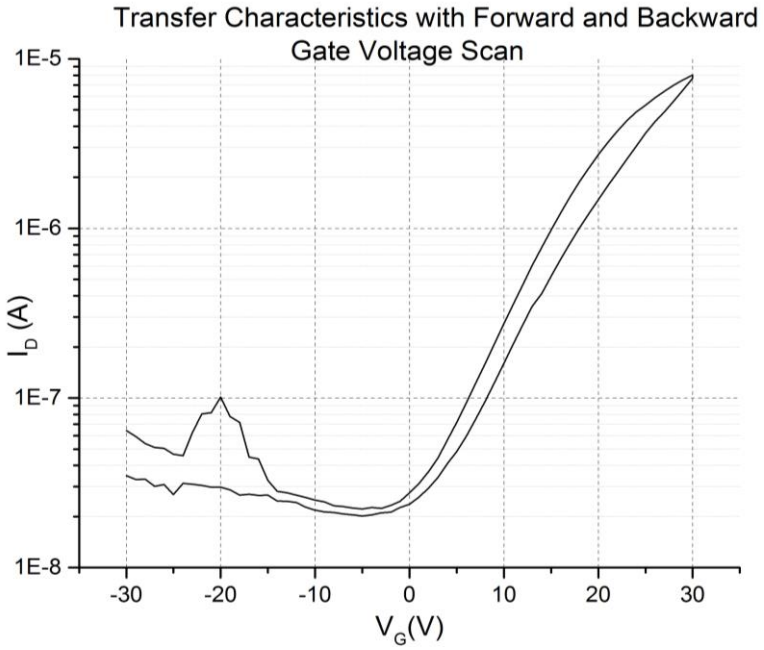


Figure 62: Transfer Characteristics with forward and backward gate voltage scan. Small amount of hysteresis is observed.

Chapter 6: Conclusion and Future Work

In this project, the thin film transistors were fabricated according to industrial parameters to switch and drive OLEDs. The parameters for the devices were specified by the OLED fabricators and the TFTs were then fabricated with strict adherence to those parameters. The required parameters for the segmented device were: ON current to be more than 100 µA and OFF current less than 100 nA. For the pixelated device: ON current should be more than 10 µA and the OFF current less than 100 nA. These specifications were given on the basis of the current required to light the OLED ON and OFF for particular voltage (+/- 30V).

In the first set of experiments, segmented devices were fabricated, which were used to switch 10mm x 5.5 mm OLED. The semiconductor layer was composed of amorphous Zinc Tin Oxide (ZTO) with an ionic molar concentration of 0.2M. The ZTO layer was 30 nm thick. The Aluminium source and drain terminals were deposited using hard masks in thermal evaporator. The dielectric used was PVP-co-PMMA with dielectric coefficient of 4.1 with a thickness of 150 nm [44]. For the gate electrode again aluminium was used and deposited in thermal evaporator by hard masks. The average ON current reached 100 µA. The leakage current and the OFF currents were 1-10 µA and 10-100 nA respectively. The majority of devices had a threshold voltage and ON/OFF ratio of 4V-6V and ~ 10^4 respectively. The mobility achieved was about 2-4 cm^2/V-s. Using these devices, OLEDs of 55 mm^2 were switched using a drain voltage of 20V and gate voltage square waveform of 0V minima and 10V maxima.

In the second set of experiments, pixelated devices were fabricated, which were to switch pixel sized OLEDs. The transistors parameters like threshold voltage, ON/OFF ratio and such were achieved by making various optimizations. For the pixelated TFTs, photolithography was also used to replace the hard mask process that was used in the fabricating segmented device. Hence the number of process steps in this case increased leading to more complexity.

The semiconductor used was amorphous ZTO (0.4M) spin coated on Quartz wafer and annealed at 773K for 60 minutes. Photolithography was then done in order to make source and drain masks. The Aluminium was deposited the same way as done for the segmented TFT. Subsequently lift-off was done to create the source and the drain terminals. The dielectric used was PVP-PMMA with PMF as cross-linking agent to improve the adhesion and reduce the leakage. It was annealed at 423 K for 60 minutes to initiate the reactions leading to cross-linking. The Photolithography was done again to make the gate mask. Thermal evaporation was used to deposit Aluminium for Gate electrode and then lift-off was completed to obtain the gate structure. The final pixelated device gave an ON current of about 11-13 µA at 30V V_G and V_D. The OFF current was less than 100 nA and the leakage current was less than 1 µA at 30V V_G and V_D. The device W/L was 890/100 µm. the minimum amount of current required to switch on OLED was more than 5 µA, and hence the ON current by pixelated TFT satisfied the conditions. All the devices were also tested for stability after running multiple cycles of characterizing and the change in the characteristics was negligible. Hence the devices were stable. Also the effect of environment was negligible up to certain extent (few days), but later some variations were observed in the transistor plots. This was due to exposure of the semiconductor layer to Oxygen, making it more conducting and increasing the OFF current.

Hence the industrial requirements for both the segmented and the pixelated devices were met. The current fabrication process included a transparent but rigid substrate (Quartz) and the fabrication temperature was high (773 K). Also the source, drain and the gate electrodes were made by Aluminium, which is opaque and the work function is not perfect to align with conductive oxides in use.

These are a few problems that are still required to be optimized. The substrate for the TFT can be transparent and at the same time flexible too like PET, which can lead to increase in the number of applications where these TFTs can be used. If the devices can be fabricated on PET like substrates then they can be used in medical sensors, skin sensors, for flexible display technology etc. The other area of optimization will be reduction in the annealing temperature of the semiconductor material. Currently this temperature for ZTO is 773 K, which is very high for any flexible substrate to be used for TFT. If this temperature is lowered till 423 K, then a lot of new substrate

options will be available and also the cost of fabrication process will reduce because of the use of low temperature. Finally the use of Aluminium as electrodes for source, drain and the gate terminals limit its application as a totally transparent device. For the currently fabricated device, the substrate, semiconductor and the dielectric all are transparent except the electrodes. If we can make use of materials like ITO or IZTO to fabricate conductive electrodes with good performance as a conductor then the possibility of making a complete transparent device will increase a lot. This will further increase the areas of application this TFT can be used, and hence there are some research areas that can be worked on in the near future.

Moreover, simple circuits including inverters, ring oscillators and logic gates can also be fabricated as next level for the development to obtain higher level of circuitry. These circuits can be used for flexible devices, sensor applications, smart clothing and in other similar areas. These circuits will also be included for applications like low cost disposable electronics, RFID tags, smart labels, etc. Other challenges will include device operations in harsh climates and environments, temperature stability, printability and scaling up of the devices.

Despite their good performance and promising future applications, these devices need more research to make them industrialized and a low cost product. These are the few areas where there is possibility of improvement in device performance, large area fabrication, stability performance etc. More investment in them in terms of finance and time, will certainly improve the practicability and we will also be able to see these devices more and more in our daily working environment.

Appendix

MATLAB Codes for Statistics Calculations

- Capacitance Calculation

```
function C=capasitance(thickness,espsilon_r)
      % calculate capasitance
      % thickness in meter;
      % epsilon_air=1;
      % epsilon_sio2=3.9;
      % epsilon_sin=7.5;
      epsilon_0=8.854e-12;%[F/m]
      C=espsilon_r*epsilon_0*1e-4/thickness;%[F/cm2] capasitance
end
```

- Linear Mobility [45]

```
function mu=mobcalclin(W,L,C,vd,vg,id)
      %idsmooth=abs(smooth(id,0.5,'rloess'));% smooth id curve
      %mob=smooth(L/(C*W*vd)*gradient(idsmooth)./gradient(vg));%[cm2/Vs]
      absid=abs(id);
      mob=L/(C*W*vd)*gradient(absid)./gradient(vg);%[cm2/Vs]
      mu=(abs(mob));
end
```

- Saturation Mobility [45]

```
function mu=mobcalcsat(W,L,C,vg,id)
      idsmooth=abs(id);%abs(smooth(id,0.5,'rloess'));% smooth id curve
      mob=smooth(2*L/(W*C)*(gradient(sqrt(idsmooth))./gradient(vg)).^2);
      mu=mob;
      %mu=(abs(mob));
end
```

- ON/OFF Ratio

```
absid=abs(id);
sqrtid=sqrt(absid);
diffsqrtid=gradient(sqrtid)./gradient(vg);

mu=mobcalcsat(W,L,C,vg,id);
figure(1)
plot(vg,mu) %Gate voltage vs mobility
figure(2)
plot(vg,sqrtid)
set(gca,'XTick',vg)
figure(3)
semilogy(vg,absid) %Semilog plot
onoff=max(absid)/min(absid) %ON/OFF ratio
W/L
```

XRD for Zinc Tin Oxide (ZTO)

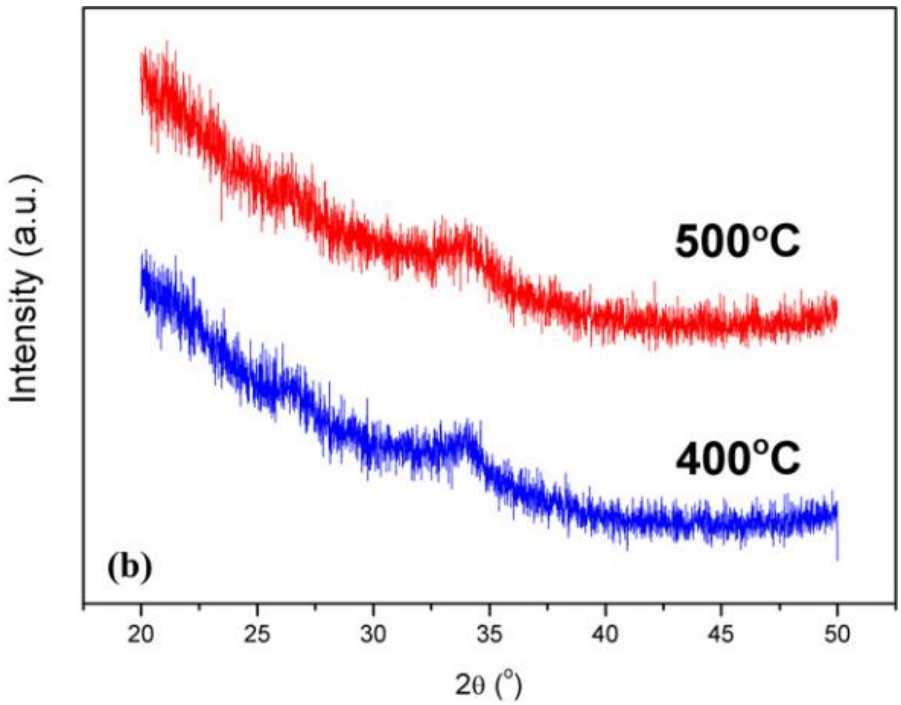


Figure 63: XRD Analysis of ZTO film at two different temperatures [46]

The X-Ray Diffraction data shown above gives two different curves at temperatures 673 K and 773 K. In both the curves a small peak can be seen at θ = 34°, implying the amorphous nature of Zinc Tin Oxide layer [46, 47].

List of Tools Used

1. Plasma Cleaner
2. Apex Instruments Co. “spinNXG - P1”
3. Thermal Evaporator
4. Keithley Semiconductor Characterization System (SCS) 4200-SCS
5. Lake Shore Cryotronics, Inc. TTP4 Probe Station
6. Karl Suss MJB4 Mask Aligner
7. Origin Pro
8. MATLAB

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“The snake which cannot cast its skin has to die.
As well the minds which are prevented from
changing their opinions; they cease to be mind.”
— Friedrich Nietzsche